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(54) **RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT**

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H03M 13/00 (2006.01)

(52) **U.S. Cl.** **714/774**; 714/784; 375/222

(58) **Field of Classification Search** 709/215; 375/222; 714/774, 784; 711/147, 153, 157, 711/170, 173; 379/93.01
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,337,877	B1	1/2002	Cole et al.	
6,707,822	B1 *	3/2004	Fadavi-Ardekani et al.	370/395.5
6,775,320	B1	8/2004	Tzannes et al.	
6,778,589	B1	8/2004	Ishii	
6,778,596	B1	8/2004	Tzannes	
2003/0067877	A1	4/2003	Sivakumar et al.	
2004/0114536	A1	6/2004	O'Rourke	
2005/0180323	A1	8/2005	Beightol et al.	
2009/0300450	A1	12/2009	Tzannes	

FOREIGN PATENT DOCUMENTS

EP	1225735	7/2002
EP	1246409	10/2002
WO	WO 03/063060 A	7/2003
WO	WO 2006/044227	4/2006

OTHER PUBLICATIONS

International Application WO 2006/04427 A1, published on Apr. 27, 2006.

PCT/US2005/036015—International Search Report, mailed Feb. 8, 2006.

http://www.sunrisetelecom.com/technotes/APP-xDSL-8B.pdf, "Sunset xDSL: Prequalification of ADSL Circuits with ATU-C Emulation" 2001, p. 3, Sunrise Telecom Inc., Application Series, San Jose, USA, XP002363272.

(Continued)

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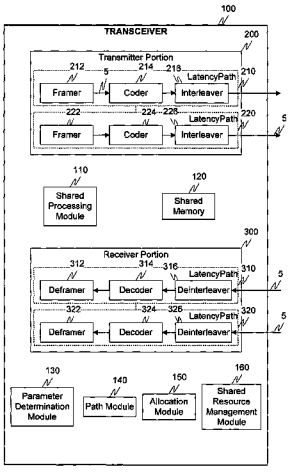
(57) **ABSTRACT**

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

8 Claims, 3 Drawing Sheets



OTHER PUBLICATIONS

Written Opinion for International (PCT) Patent Application No. PCT/US2005/036015, mailed Feb. 8, 2006.

International Preliminary Report on Patentability for International (PCT) Patent Application No. PCT/US2005/036015, mailed Apr. 26, 2007.

Examiner's First Report for Australian Patent Application No. 2005296086, mailed Jun. 24, 2009.

Notification of the First Office Action (including translation) for Chinese Patent Application No. 200580032703, mailed Sep. 25, 2009.

Shoji, T. et al: "Wireless Access Method to Ensure Each Users QOS in Unpredictable and Various QOS Requirements Wireless Personal Communications," Springer, Dordrecht, NL, vol. 22, No. 2, Aug. 2002, pp. 139-151.

"ITU-T Recommendation G.992.5—Series G: Transmission Systems and Media, Digital Systems and Networks", International Telecommunication Union, ADSL2, May 2003, 92 pages.

U.S. Appl. No. 12/783,758, filed May 20, 2010, Tzannes.

U.S. Appl. No. 12/760,728, filed Apr. 15, 2010, Tzannes.

U.S. Appl. No. 12/783,765, filed May 20, 2010, Tzannes.

U.S. Appl. No. 12/761,586, filed Apr. 16, 2010, Lund et al.

"ITU-T Recommendation G.992.3," International Telecommunication Union, ADSL2, Jan. 2005, 436 pages.

"VDSL2 ITU-T Recommendation G.993.2," International Telecommunication Union, Feb. 2006, 252 pages.

* cited by examiner

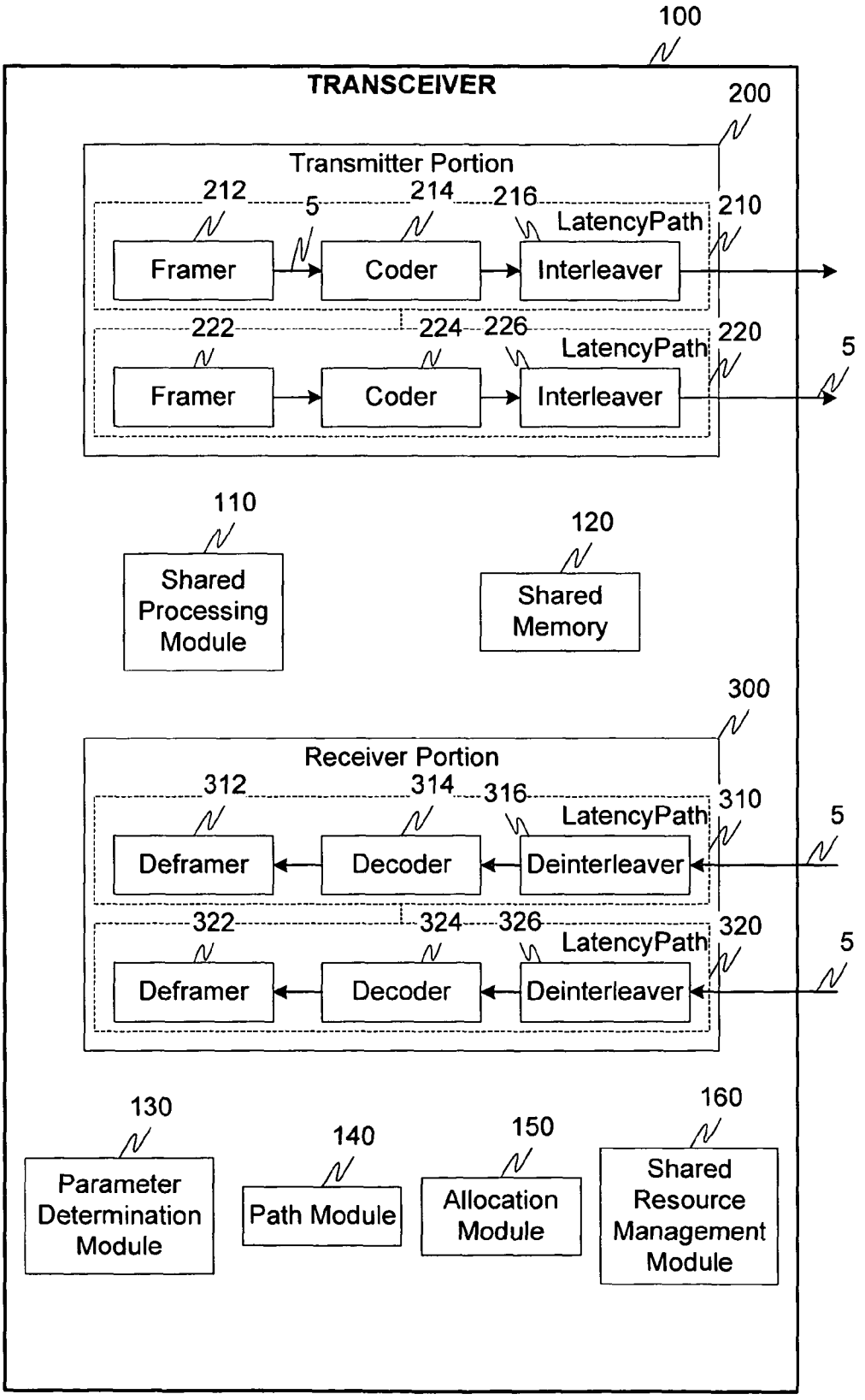

100
TRANSCEIVER
200
Transmitter Portion
212
5
214
216
LatencyPath
210
Framer
Coder
Interleaver
222
224
226
LatencyPath
220
5
Framer
Coder
Interleaver
110
Shared Processing Module
120
Shared Memory
300
Receiver Portion
312
314
316
LatencyPath
310
5
Deframer
Decoder
Deinterleaver
322
324
326
LatencyPath
320
5
Deframer
Decoder
Deinterleaver
130
Parameter Determination Module
140
Path Module
150
Allocation Module
160
Shared Resource Management Module

Fig. 1

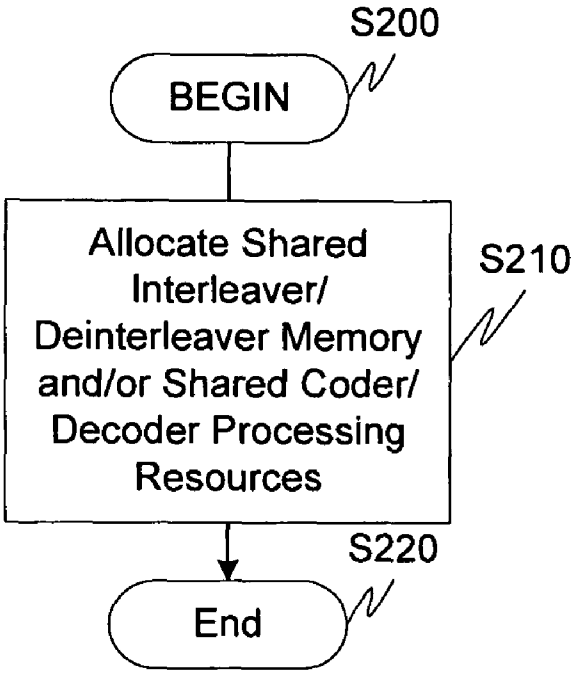

S200
BEGIN
Allocate Shared Interleaver/ Deinterleaver Memory and/or Shared Coder/ Decoder Processing Resources
S210
S220
End

Fig. 2

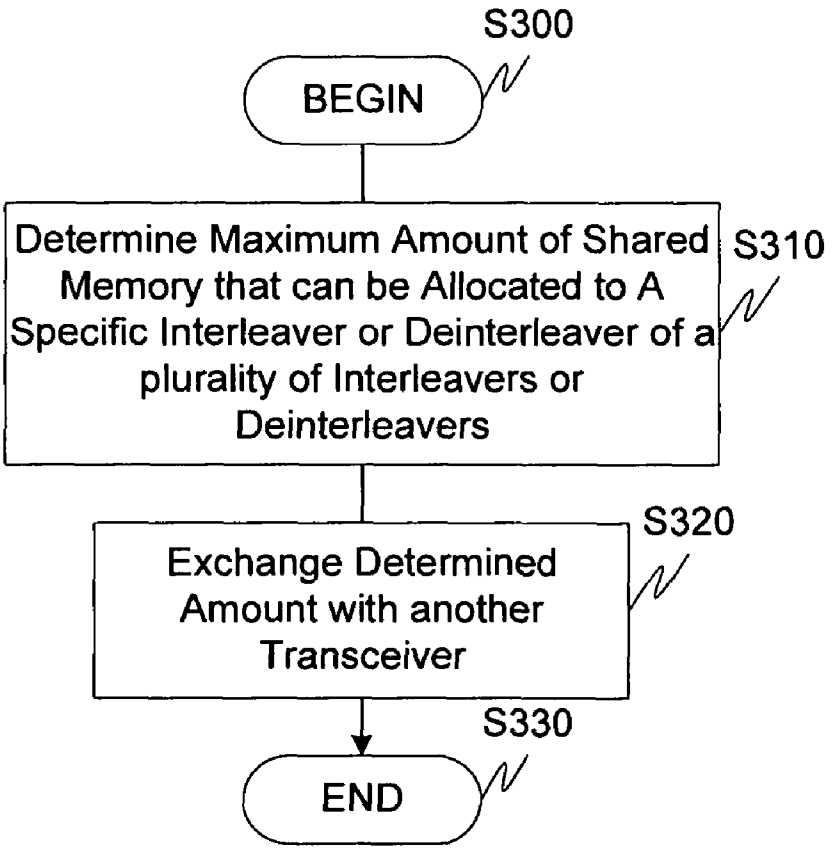

S300
BEGIN
Determine Maximum Amount of Shared Memory that can be Allocated to A Specific Interleaver or Deinterleaver of a plurality of Interleavers or Deinterleavers
S310
Exchange Determined Amount with another Transceiver
S320
S330
END

Fig. 3

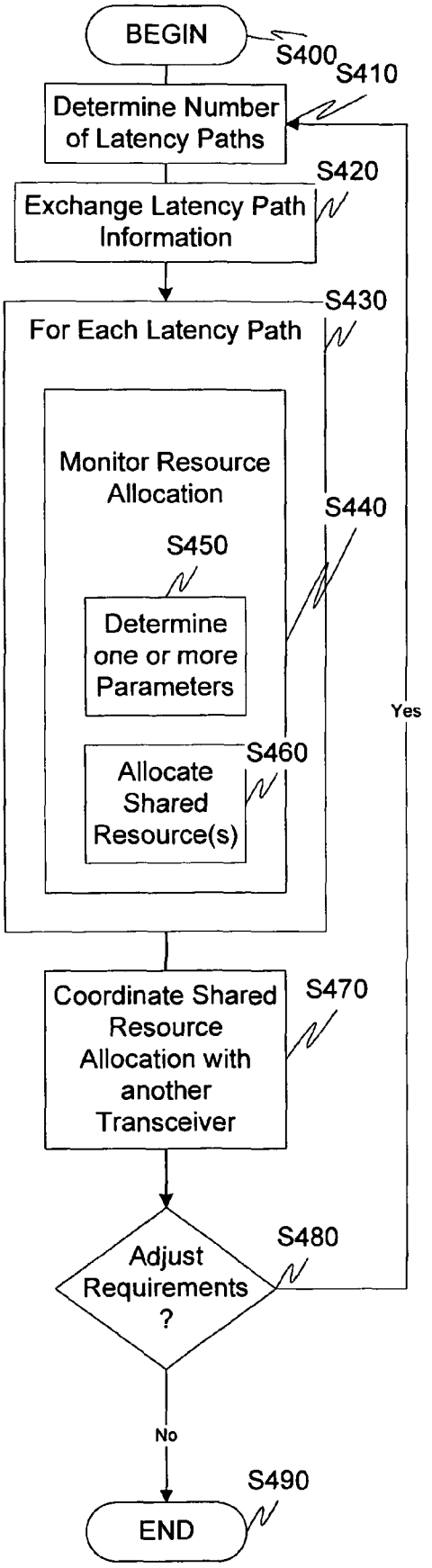

BEGIN
S400
S410
Determine Number of Latency Paths
S420
Exchange Latency Path Information
S430
For Each Latency Path
Monitor Resource Allocation
S440
S450
Determine one or more Parameters
S460
Allocate Shared Resource(s)
Yes
S470
Coordinate Shared Resource Allocation with another Transceiver
S480
Adjust Requirements ?
No
S490
END

Fig. 4

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

This application claims the benefit of and priority under 35 U.S.C. §119(e) to U.S. Patent Application No. 60/618,269, filed Oct. 12, 2004, entitled "Sharing Memory and Processing Resources in DSL Systems," which is incorporated herein by reference in its entirety.

BACKGROUND

1. Field of the Invention

This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

2. Description of Related Art

U.S. Pat. Nos. 6,775,320 and 6,778,589 describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

As described in U.S. Pat. No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a combination thereof and a shared memory designed to be allocated to a plurality of the modules.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

FIG. **1** is a functional block diagram illustrating an exemplary transceiver according to this invention;

FIG. **2** is a flowchart outlining an exemplary method of sharing resources according to this invention;

FIG. **3** is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

FIG. **4** is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used interchangeably.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100** that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver **100** can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to-determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100**. The transceiver **100** includes a transmitter portion **200** and a receiver portion **300**. The transmitter portion **200** includes one or more latency paths **210**, **220**, ... Similarly, the receiver portion **300** includes one or more latency paths **310**, **320**, ... Each of the latency paths in the transmitter portion **200** includes a framer, coder, and interleaver designated as **212**, **214**, **216** and **222**, **224** and **226**, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as **312**, **314**, **316** and **322**, **324**, and **326**, respectively. The transceiver **100** further includes a shared processing module **110**, a shared memory **120**, a parameter determination module **130**, a path module **140**, an allocation module **150**, and a shared resource management module **160**, all interconnected by one or more links (not shown).

In this exemplary embodiment, the transceiver **100** is illustrated with four total transmitter portion and receiver portion latency paths, i.e., **210**, **220**, **310**, and **320**. The shared memory **120** is shared amongst the two transmitter portion interleavers **216** and **226** and two receiver portion deinterleavers **316** and **326**. The shared processing module **110**, such as a shared coding module, is shared between the two transmitter portion coders **214** and **224** and the two receiver portion decoders **314** and **324**.

While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of

transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path **210**, the interleaver **216** could be allocated a portion of the shared memory **120**, while the coder **214** could be allocated to a dedicated processing module, vice versa, or the like.

In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory **120**, and a coding module, such as shared processing module **110**. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module **110**, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory **120** to an interleaver, such as interleaver **216** in the transmitter portion of the transceiver and allocate a second portion of the shared memory **120** to a deinterleaver, such as **316**, in the receiver portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory **120**, and be designed to allocate a first portion of shared memory **120** to a first interleaver, e.g., **216**, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., **226**, in the transmitter portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory **120** to a first deinterleaver, e.g., **316**, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., **326**, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory **120**.

Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module **140**, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module **130** then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module **150** allocates a portion of the shared memory **120** to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management **160**, the transceiver **100** transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

EXAMPLE #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64(D=64). This latency path will require N*D=255*64=16Kbytes of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

A second transmitter portion or receiver portion latency path may carry an internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). This latency path will require N*D=128*32=4 Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least (16+4)=20 Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with N=255/R=16 and N=128/R=8.

According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in

ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

EXAMPLE #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes.(N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). Each latency path will require N*D=128*32=4 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with N=128/R=16, N=128/R=8 and N=128/R=8.

EXAMPLE #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only 2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes (N=200) with 10 checkbytes (R=10) and interleaving/deinterleaving using an interleaver depth of 50 (D=50). Each latency path will require N*D=200*50=10 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g, N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

Number of supported transmitter and receiver latency paths=3
Max Interleaver Memory for latency path #1=16 Kbytes
Max Interleaver Memory for latency path #2=16 Kbytes
Max Interleaver Memory for latency path #3=16 Kbytes
Maximum total/shared memory for all latency paths=20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1—Video: N=255, R=16, D=64
latency path #2—Video: N=128, R=8, D=32
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would result in a total interleaver memory of 20 kbytes.

Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1—Video: N=200, R=10, D=50
latency path #2—Video: N=200, R=10, D=50
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would also result in a total interleaver memory of 20 kbytes.

Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

FIG. **2** outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step S**200** and continues to step S**210**. In step S**210**, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S**220** where the control sequence ends.

FIG. **3** outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S**310**. In step S**310**, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S**320**, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing addi-

tional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S**330** where the control sequence ends.

FIG. **4** outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S**400** and continues to step S**410**. In step S**410**, the number of latency paths are determined. Then, in step S**420**, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S**430**.

In step S**430**, and for each latency path, the steps in step **440** are performed.

In step S**440**, and while monitoring of allocation of resources is being performed, steps **450** and **460** are performed. More specifically, in step S**450**, one or more parameters associated with the communication system are determined. Then, in step S**460**, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S**470**.

In step S**470**, the allocation of shared resources is communicated to another transceiver. Next, in step S**480**, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S**410**. Otherwise, control jumps to step S**490** where the control sequence ends.

The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

The invention claimed is:

1. A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

determining, at the transceiver, an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating, in the transceiver, a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

2. The method of claim **1**, wherein the determining is based on an impulse noise protection requirement.

3. The method of claim 1, wherein the determining is based on a latency requirement.

4. The method of claim 1, wherein the determining is based on a bit error rate requirement.

5. A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shred memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

6. The method of claim 5, wherein the determining is based on an impulse noise protection requirement.

7. The method of claim 5, wherein the determining is based on a latency requirement.

8. The method of claim 5, wherein the determining is based on a bit error rate requirement.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,831,890 B2
APPLICATION NO. : 11/246163
DATED : November 9, 2010
INVENTOR(S) : Marcos C. Tzannes et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

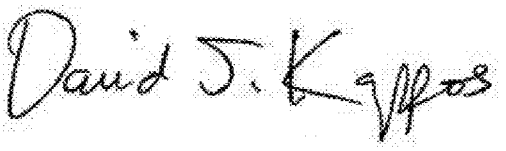
ln the claims:

ln column 11, claim 5, line 18, delete “transmission” and insert -- reception --

ln column 12, claim 5, line 3, delete “received” and insert -- transmitted --

ln column 12, claim 5, line 8, delete “shred” and insert -- shared --

Signed and Sealed this
Eighth Day of February, 2011



David J. Kappos
Director of the United States Patent and Trademark Office

US007836381B1

(12) **United States Patent**
Tzannes et al.

(10) **Patent No.: US 7,836,381 B1**
(45) **Date of Patent: *Nov. 16, 2010**

(54) **COMPUTER READABLE MEDIUM WITH INSTRUCTIONS FOR RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT**

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(73) Assignee: **Aware, Inc.**, Bedford, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **12/853,020**

(22) Filed: **Aug. 9, 2010**

Related U.S. Application Data

(63) Continuation of application No. 11/246,163, filed on Oct. 11, 2005.

(60) Provisional application No. 60/618,269, filed on Oct. 12, 2004.

(51) **Int. Cl.**
H03M 13/00 (2006.01)

(52) **U.S. Cl.** **714/774**; 714/784; 375/222

(58) **Field of Classification Search** 709/215; 375/222; 714/774, 784; 711/147, 153, 157, 711/170, 173; 379/93.01
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,337,877	B1	1/2002	Cole et al.	
6,707,822	B1 *	3/2004	Fadavi-Ardekani et al.	370/395.5
6,775,320	B1	8/2004	Tzannes et al.	
6,778,589	B1	8/2004	Ishii	
6,778,596	B1	8/2004	Tzannes	
2003/0067877	A1	4/2003	Sivakumar et al.	
2004/0114536	A1	6/2004	O'Rourke	
2005/0180323	A1	8/2005	Beightol et al.	
2006/0088054	A1	4/2006	Tzannes et al.	
2009/0300450	A1	12/2009	Tzannes	

FOREIGN PATENT DOCUMENTS

EP	1225735	7/2002
EP	1246409	10/2002
WO	WO 03/063060	7/2003
WO	WO 2006/044227	4/2006

OTHER PUBLICATIONS

U.S. Appl. No. 12/783,758, filed May 20, 2010, Tzannes.
U.S. Appl. No. 12/760,728, filed Apr. 15, 2010, Tzannes.
U.S. Appl. No. 12/783,765, filed May 20, 2010, Tzannes.

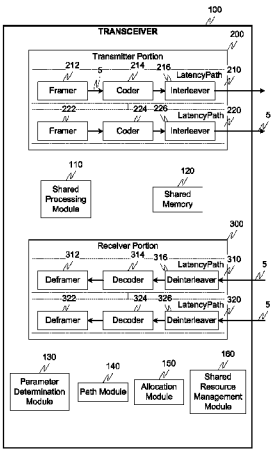
(Continued)

Primary Examiner—Joon H Hwang
Assistant Examiner—Mark Pfizenmayer
(74) *Attorney, Agent, or Firm*—Jason H. Vick; Sheridan Ross P.C.

(57) **ABSTRACT**

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

8 Claims, 3 Drawing Sheets



OTHER PUBLICATIONS

U.S. Appl. No. 12/761,586, filed Apr. 16, 2010, Lund et al.

Shoji, T. et al: "Wireless Access Method to Ensure Each Users QOS in Unpredictable and Various QOS Requirements Wireless Personal Communications," Springer, Dordrecht, NL, vol. 22, No. 2, Aug. 2002, pp. 139-151.

"ITU-T Recommendation G.992.5—Series G: Transmission Systems and Media, Digital Systems and Networks", International Telecommunication Union, ADSL2, May 2003, 92 pages.

"ITU-T Recommendation G.992.3," International Telecommunication Union, ADSL2, Jan. 2005, 436 pages.

"VDSL2 ITU-T Recommendation G.993.2," International Telecommunication Union, Feb. 2006, 252 pages.

"Sunset xDSL: Prequalification of ADSL Circuits with ATU-C Emulation," Sunrise Telecom Inc., Application Series, 2001, San Jose, USA, p. 3, available at http://www.sunrisetelecom.com/technotes/APP-xDSL-8B.pdf.

International Search Report for International (PCT) Patent Application No. PCT/US2005/036015, mailed Feb. 8, 2006.

Written Opinion for International (PCT) Patent Application No. PCT/US2005/036015, mailed Feb. 8, 2006.

International Preliminary Report on Patentability for International (PCT) Patent Application No. PCT/US2005/036015, mailed Apr. 26, 2007.

Examiner's First Report for Australian Patent Application No. 2005296086, mailed Jun. 24, 2009.

Notification of the First Action (including translation) for Chinese Patent Application No. 200580032703, mailed Sep. 25, 2009.

Official Action for U.S. Appl. No. 11/246,163, mailed Feb. 24, 2009.

Official Action for U.S. Appl. No. 11/246,163, mailed Dec. 9, 2009.

* cited by examiner

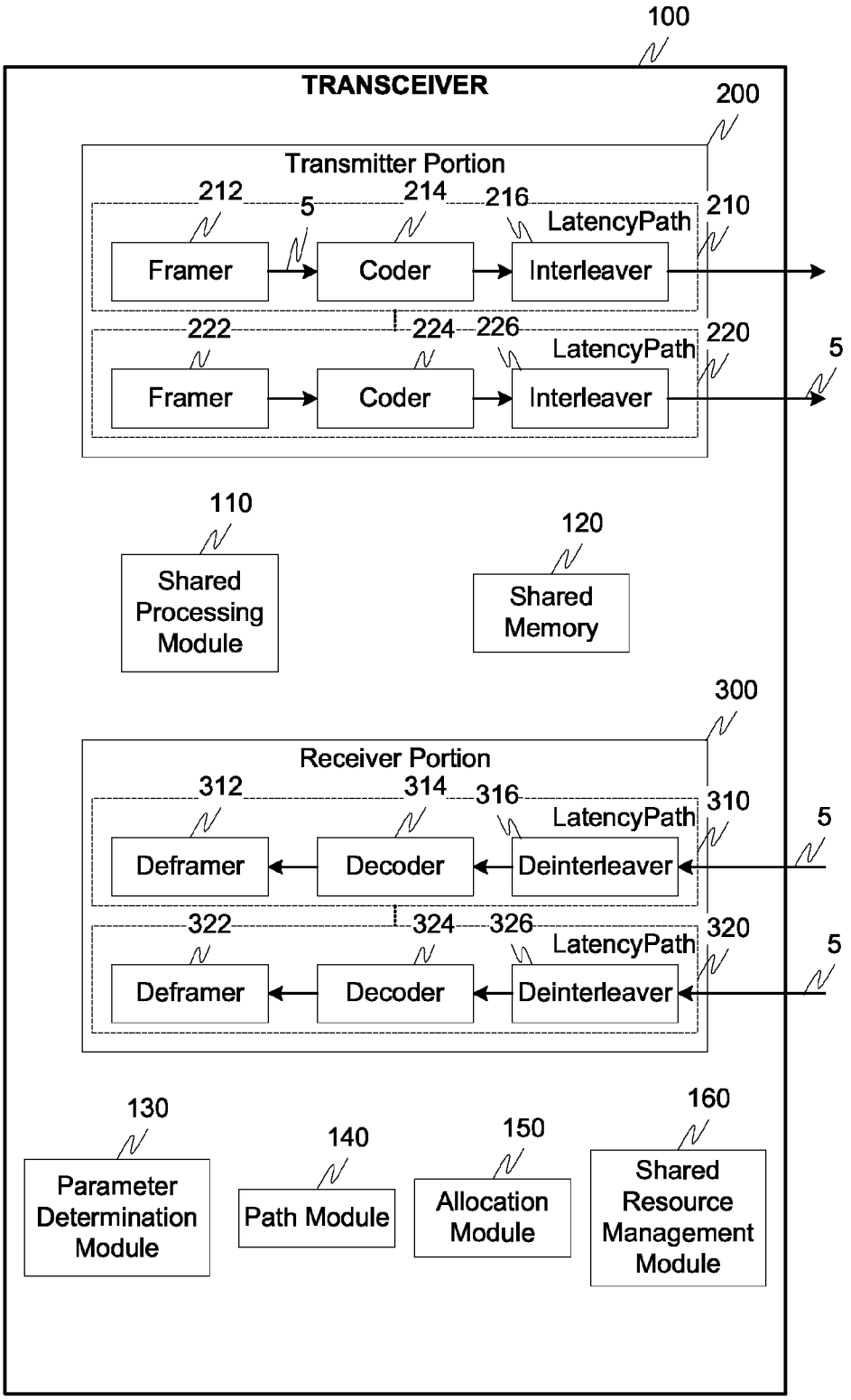

100
TRANSCEIVER
200
Transmitter Portion
212
5
214
216
LatencyPath
210
Framer
Coder
Interleaver
222
224
226
LatencyPath
220
5
Framer
Coder
Interleaver
110
Shared Processing Module
120
Shared Memory
300
Receiver Portion
312
314
316
LatencyPath
310
5
Deframer
Decoder
Deinterleaver
322
324
326
LatencyPath
320
5
Deframer
Decoder
Deinterleaver
130
Parameter Determination Module
140
Path Module
150
Allocation Module
160
Shared Resource Management Module

Fig. 1

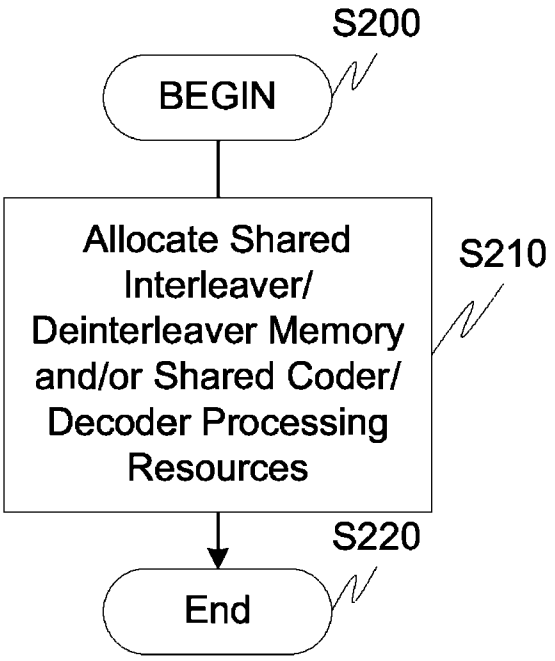

S200
BEGIN
Allocate Shared Interleaver/ Deinterleaver Memory and/or Shared Coder/ Decoder Processing Resources
S210
S220
End

Fig. 2

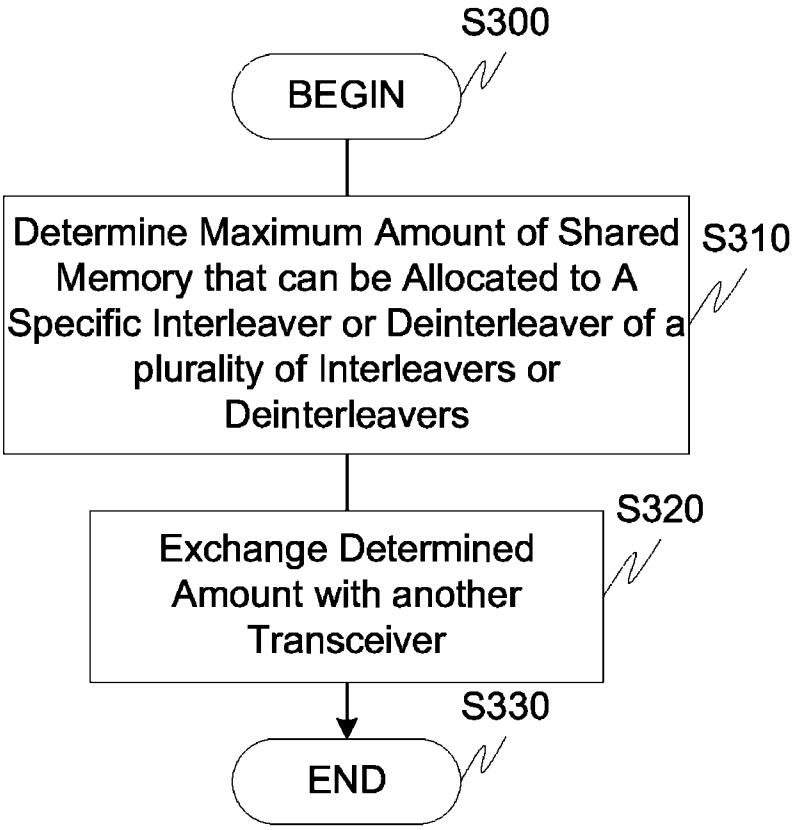

S300
BEGIN
Determine Maximum Amount of Shared Memory that can be Allocated to A Specific Interleaver or Deinterleaver of a plurality of Interleavers or Deinterleavers
S310
Exchange Determined Amount with another Transceiver
S320
S330
END

Fig. 3

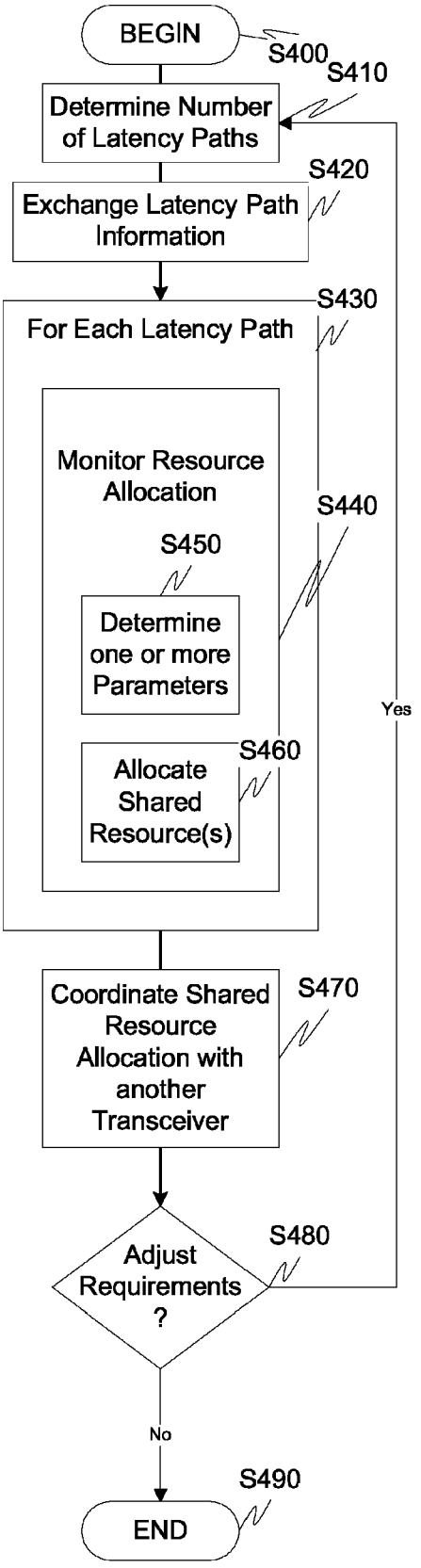

BEGIN
S400
S410
Determine Number of Latency Paths
S420
Exchange Latency Path Information
S430
For Each Latency Path
Monitor Resource Allocation
S440
S450
Determine one or more Parameters
S460
Allocate Shared Resource(s)
Yes
S470
Coordinate Shared Resource Allocation with another Transceiver
S480
Adjust Requirements ?
No
S490
END

Fig. 4

COMPUTER READABLE MEDIUM WITH INSTRUCTIONS FOR RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

This application is a Continuation of U.S. application Ser. No. 11/246,163 filed Oct. 11, 2005, which claims the benefit of and priority under 35 U.S.C. §119(e) to U.S. Patent Application No. 60/618,269, filed Oct. 12, 2004, entitled "Sharing Memory and Processing Resources in DSL Systems," each of which are incorporated herein by reference in their entirety.

BACKGROUND

1. Field of the Invention

This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

2. Description of Related Art

U.S. Pat. Nos. 6,775,320 and 6,778,589 describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

As described in U.S. Pat. No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a combination thereof and a shared memory designed to be allocated to a plurality of the modules.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

FIG. **1** is a functional block diagram illustrating an exemplary transceiver according to this invention;

FIG. **2** is a flowchart outlining an exemplary method of sharing resources according to this invention;

FIG. **3** is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

FIG. **4** is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used interchangeably.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100** that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver **100** can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100**. The transceiver **100** includes a transmitter portion **200** and a receiver portion **300**. The transmitter portion **200** includes one or more latency paths **210**, **220**, ... Similarly, the receiver portion **300** includes one or more latency paths **310**, **320**, ... Each of the latency paths in the transmitter portion **200** includes a framer, coder, and interleaver designated as **212**, **214**, **216** and **222**, **224** and **226**, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as **312**, **314**, **316** and **322**, **324**, and **326**, respectively. The transceiver **100** further includes a shared processing module **110**, a shared memory **120**, a parameter determination module **130**, a path module **140**, an allocation module **150**, and a shared resource management module **160**, all interconnected by one or more links (not shown).

In this exemplary embodiment, the transceiver **100** is illustrated with four total transmitter portion and receiver portion latency paths, i.e., **210**, **220**, **310**, and **320**. The shared memory **120** is shared amongst the two transmitter portion interleavers **216** and **226** and two receiver portion deinterleavers **316** and **326**. The shared processing module **110**, such as a shared coding module, is shared between the two transmitter portion coders **214** and **224** and the two receiver portion decoders **314** and **324**.

While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of

transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path **210**, the interleaver **216** could be allocated a portion of the shared memory **120**, while the coder **214** could be allocated to a dedicated processing module, vice versa, or the like.

In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory **120**, and a coding module, such as shared processing module **110**. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module **110**, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory **120** to an interleaver, such as interleaver **216** in the transmitter portion of the transceiver and allocate a second portion of the shared memory **120** to a deinterleaver, such as **316**, in the receiver portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory **120**, and be designed to allocate a first portion of shared memory **120** to a first interleaver, e.g., **216**, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., **226**, in the transmitter portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory **120** to a first deinterleaver, e.g., **316**, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., **326**, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory **120**.

Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module **140**, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module **130** then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module **150** allocates a portion of the shared memory **120** to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management **160**, the transceiver **100** transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require N*D=255*64=16 Kbytes of interleaver memory at the transmitter (or deinterleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

A second transmitter portion or receiver portion latency path may carry an internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). This latency path will require N*D=128*32=4 Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least (16+4)=20 Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with N=255/R=16 and N=128/R=8.

According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in

ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). Each latency path will require N*D=128*32=4 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with N=128/R=16, N=128/R=8 and N=128/R=8.

Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only 2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes (N=200) with 10 checkbytes (R=10) and interleaving/deinterleaving using an interleaver depth of 50 (D=50). Each latency path will require N*D=200*50=10 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

Number of supported transmitter and receiver latency paths=3
Max Interleaver Memory for latency path #1=16 Kbytes
Max Interleaver Memory for latency path #2=16 Kbytes
Max Interleaver Memory for latency path #3=16 Kbytes
Maximum total/shared memory for all latency paths=20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1—Video: N=255, R=16, D=64

latency path #2—Video: N=128, R=8, D=32

latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would result in a total interleaver memory of 20 kbytes.

Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1—Video: N=200, R=10, D=50

latency path #2—Video: N=200, R=10, D=50

latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would also result in a total interleaver memory of 20 kbytes.

Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

FIG. **2** outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step **S200** and continues to step **S210**. In step **S210**, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step **S220** where the control sequence ends.

FIG. **3** outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step **S310**. In step **S310**, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plural-

ity of interleavers or deinterleavers in a transceiver is determined. Next, in step S**320**, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S**330** where the control sequence ends.

FIG. **4** outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S**400** and continues to step S**410**. In step S**410**, the number of latency paths are determined. Then, in step S**420**, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S**430**.

In step S**430**, and for each latency path, the steps in step **440** are performed.

In step S**440**, and while monitoring of allocation of resources is being performed, steps **450** and **460** are performed. More specifically, in step S**450**, one or more parameters associated with the communication system are determined. Then, in step S**460**, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S**470**.

In step S**470**, the allocation of shared resources is communicated to another transceiver. Next, in step S**480**, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S**410**. Otherwise, control jumps to step S**490** where the control sequence ends.

The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

The invention claimed is:

1. A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

determining, at the transceiver, an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating, in the transceiver, a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data

bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

2. The media of claim **1**, wherein the determining is based on an impulse noise protection requirement.

3. The media of claim **1**, wherein the determining is based on a latency requirement.

4. The media of claim **1**, wherein the determining is based on a bit error rate requirement.

5. A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shred memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

6. The media of claim **5**, wherein the determining is based on an impulse noise protection requirement.

7. The media of claim **5**, wherein the determining is based on a latency requirement.

8. The media of claim **5**, wherein the determining is based on a bit error rate requirement.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,836,381 B1
APPLICATION NO. : 12/853020
DATED : November 16, 2010
INVENTOR(S) : Marcos C. Tzannes et al.

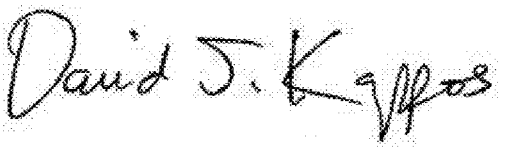
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

ln column 12, claim 5, line 2, delete “transmission” and insert -- reception --

ln column 12, claim 5, line 7, delete “received” and insert -- transmitted --

ln column 12, claim 5, line 12, delete “shred” and insert -- shared --

Signed and Sealed this
Eighth Day of February, 2011



David J. Kappos
Director of the United States Patent and Trademark Office

US007844882B2

(12) **United States Patent**
Tzannes et al.

(10) **Patent No.: US 7,844,882 B2**
(45) **Date of Patent: *Nov. 30, 2010**

(54) **RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT**

(75) Inventors: **Marcos C. Tzannes**, Orinda, CA (US); **Michael Lund**, West Newton, MA (US)

(73) Assignee: **Aware, Inc.**, Bedford, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **12/761,586**

(22) Filed: **Apr. 16, 2010**

(65) **Prior Publication Data**

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Related U.S. Application Data

(63) Continuation of application No. 11/246,163, filed on Oct. 11, 2005.

(60) Provisional application No. 60/618,269, filed on Oct. 12, 2004.

(51) **Int. Cl.**
H03M 13/00 (2006.01)

(52) **U.S. Cl.** **714/774**; 714/784; 375/222

(58) **Field of Classification Search** 709/215; 375/222; 714/774, 784; 711/147, 153, 157, 711/170, 173; 379/93.01
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,337,877	B1	1/2002	Cole et al.	
6,707,822	B1 *	3/2004	Fadavi-Ardekani et al.	370/395.5
6,775,320	B1	8/2004	Tzannes et al.	
6,778,589	B1	8/2004	Ishii	
6,778,596	B1	8/2004	Tzannes	
2003/0067877	A1	4/2003	Sivakumar et al.	
2004/0114536	A1	6/2004	O'Rourke	
2005/0180323	A1	8/2005	Beightol et al.	
2006/0088054	A1	4/2006	Tzannes et al.	
2009/0300450	A1	12/2009	Tzannes	

FOREIGN PATENT DOCUMENTS

EP	1225735	7/2002
EP	1246409	10/2002
WO	WO 03/063060	7/2003

(Continued)

OTHER PUBLICATIONS

U.S. Appl. No. 12/783,758, filed May 20, 2010 Tzannes.

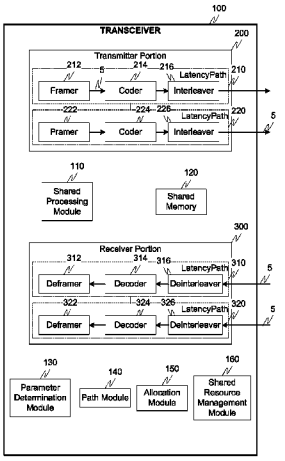
(Continued)

Primary Examiner—Joon H Hwang
Assistant Examiner—Mark Pfizenmayer
(74) *Attorney, Agent, or Firm*—Jason H. Vick; Sheridan Ross, P.C.

(57) **ABSTRACT**

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

16 Claims, 3 Drawing Sheets



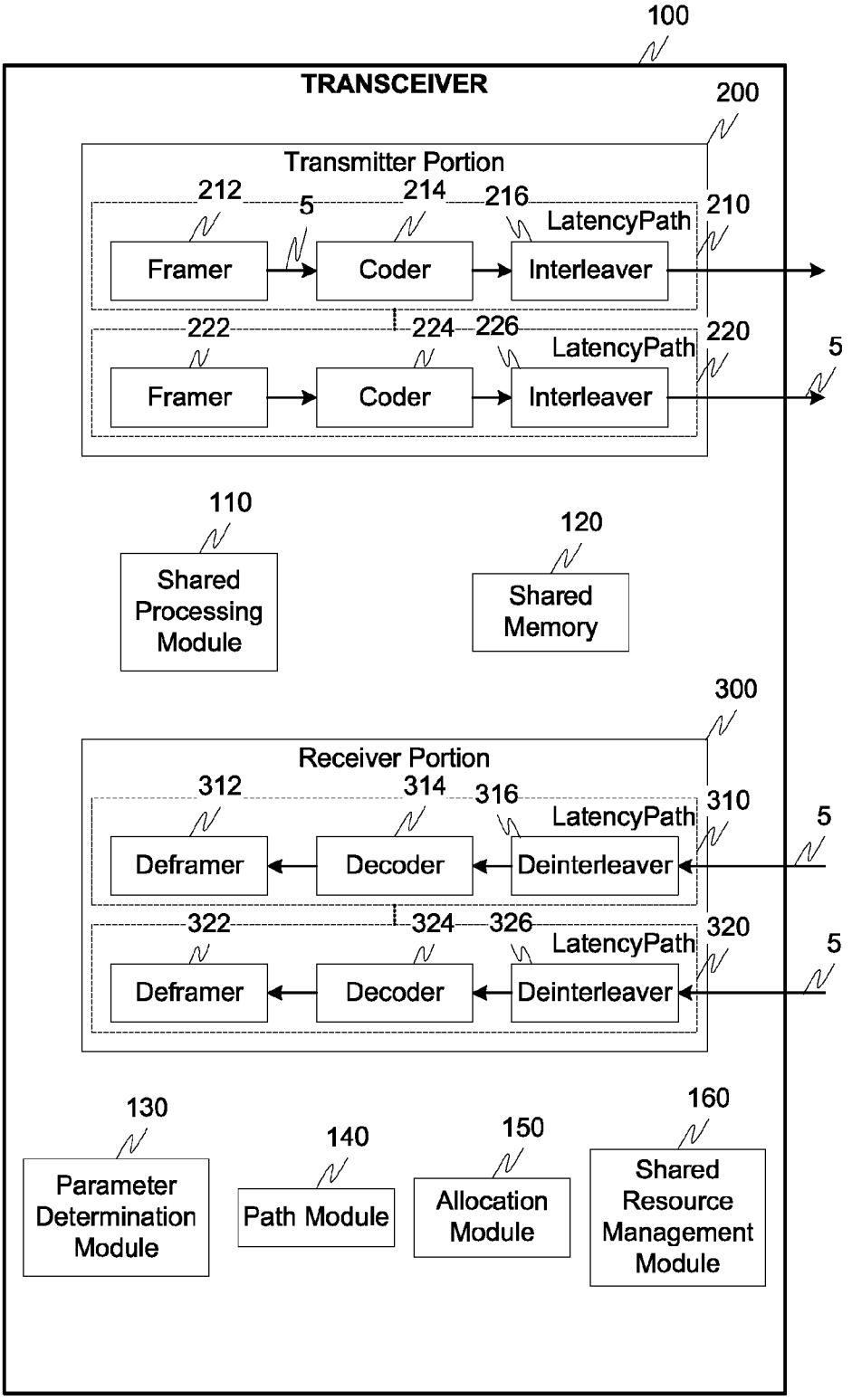
FOREIGN PATENT DOCUMENTS

WO	WO 2006/044227	4/2006

OTHER PUBLICATIONS

U.S. Appl. No. 12/760,728, filed Apr. 15, 2010 Tzannes.
U.S. Appl. No. 12/783,765, filed May 20, 2010 Tzannes.
Shoji, T. et al: "Wireless Access Method to Ensure Each Users QOS in Unpredictable and Various QOS Requirements Wireless Personal Communications," Springer, Dordrecht, NL, vol. 22, No. 2, Aug. 2002, pp. 139-151.
"ITU-T Recommendation G.992.5—Series G: Transmission Systems and Media, Digital Systems and Networks", International Telecommunication Union, ADSL2, May 2003, 92 pages.
"ITU-T Recommendation G.992.3," International Telecommunication Union, ADSL2, Jan. 2005, 436 pages.
"VDSL2 ITU-T Recommendation G.993.2," International Telecommunication Union, Feb. 2006, 252 pages.
"Sunset xDSL: Prequalification of ADSL Circuits with ATU-C Emulation," Sunrise Telecom Inc., Application Series, 2001, San Jose, USA, p. 3, available at http://www.sunrisetelecom.com/technotes/APP-xDSL-8B.pdf.
International Search Report for International (PCT) Patent Application No. PCT/US2005/036015, mailed Feb. 8, 2006.
Written Opinion for International (PCT) Patent Application No. PCT/US2005/036015, mailed Feb. 8, 2006.
International Preliminary Report on Patentability for International (PCT) Patent Application No. PCT/US2005/036015, mailed Apr. 26, 2007.
Examiner's First Report for Australian Patent Application No. 2005296086, mailed Jun. 24, 2009.
Notification of the First Office Action (including translation) for Chinese Patent Application No. 200580032703, mailed Sep. 25, 2009.
Official Action for U.S. Appl. No. 11/246,163, mailed Feb. 24, 2009.
Official Action for U.S. Appl. No. 11/246,163, mailed Dec. 9, 2009.

* cited by examiner


100
TRANSCEIVER
200
Transmitter Portion
212
5
214
216
LatencyPath
210
Framer
Coder
Interleaver
222
224
226
LatencyPath
220
5
Framer
Coder
Interleaver
110
Shared Processing Module
120
Shared Memory
300
Receiver Portion
312
314
316
LatencyPath
310
5
Deframer
Decoder
Deinterleaver
322
324
326
LatencyPath
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Deframer
Decoder
Deinterleaver
130
Parameter Determination Module
140
Path Module
150
Allocation Module
160
Shared Resource Management Module

Fig. 1

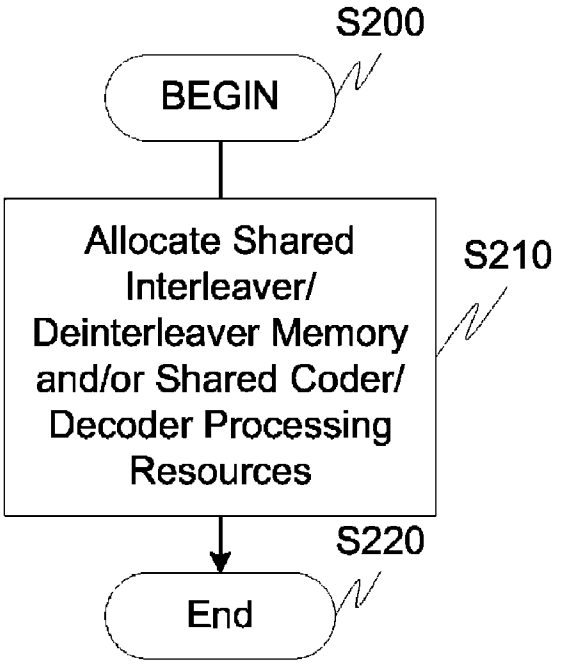

S200
BEGIN
Allocate Shared Interleaver/ Deinterleaver Memory and/or Shared Coder/ Decoder Processing Resources
S210
S220
End

Fig. 2

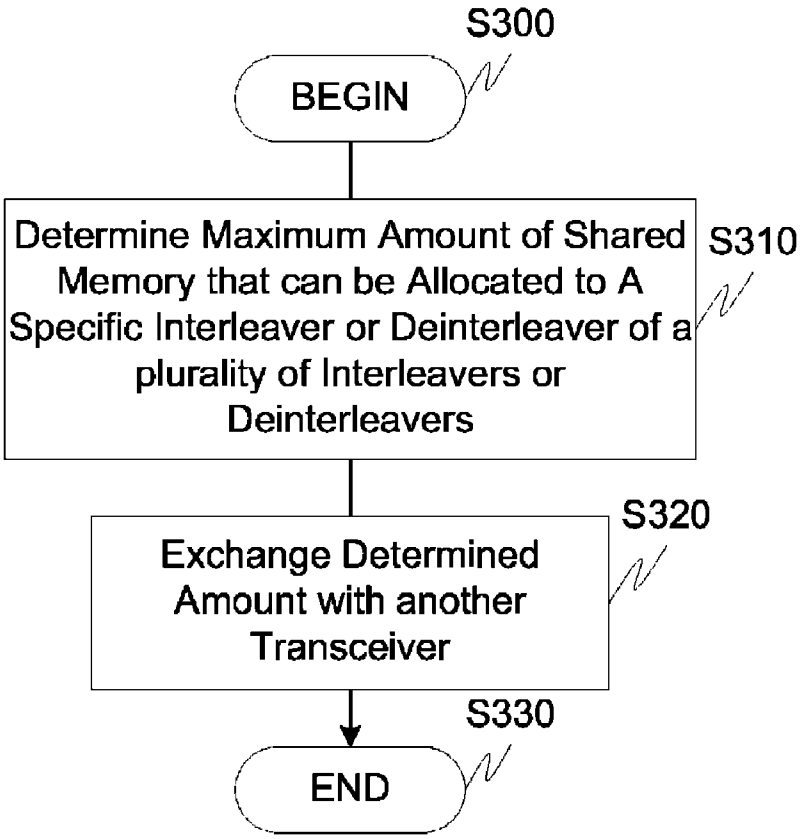

S300
BEGIN
Determine Maximum Amount of Shared Memory that can be Allocated to A Specific Interleaver or Deinterleaver of a plurality of Interleavers or Deinterleavers
S310
Exchange Determined Amount with another Transceiver
S320
S330
END

Fig. 3

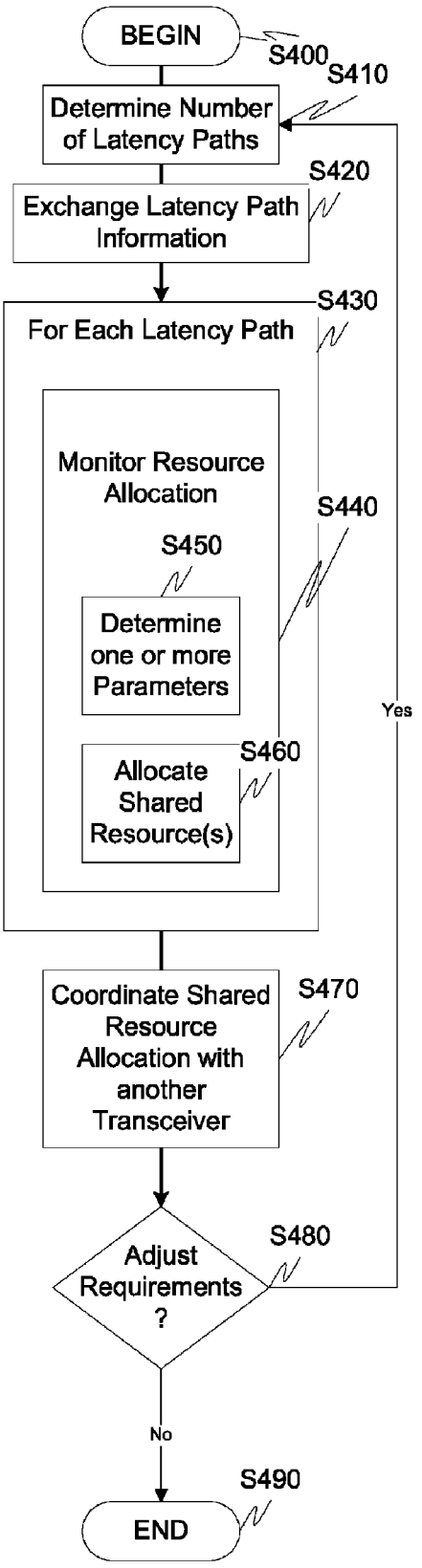

BEGIN
S400
S410
Determine Number of Latency Paths
S420
Exchange Latency Path Information
S430
For Each Latency Path
Monitor Resource Allocation
S440
S450
Determine one or more Parameters
S460
Allocate Shared Resource(s)
Yes
S470
Coordinate Shared Resource Allocation with another Transceiver
S480
Adjust Requirements ?
No
S490
END

Fig. 4

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

This application is a Continuation of U.S. application Ser. No. 11/246,163 filed Oct. 11, 2005, which claims the benefit of and priority under 35 U.S.C. §119(e) to U.S. Patent Application No. 60/618,269, filed Oct. 12, 2004, entitled "Sharing Memory and Processing Resources in DSL Systems," each of which are incorporated herein by reference in their entirety.

BACKGROUND

1. Field of the Invention

This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

2. Description of Related Art

U.S. Pat. Nos. 6,775,320 and 6,778,589 describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

As described in U.S. Pat. No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a combination thereof and a shared memory designed to be allocated to a plurality of the modules.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

FIG. **1** is a functional block diagram illustrating an exemplary transceiver according to this invention;

FIG. **2** is a flowchart outlining an exemplary method of sharing resources according to this invention;

FIG. **3** is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

FIG. **4** is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

Furthermore, it should be appreciated that the various links, including communications channel **5**, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used interchangeably.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100** that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver **100** can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100**. The transceiver **100** includes a transmitter portion **200** and a receiver portion **300**. The transmitter portion **200** includes one or more latency paths **210**, **220**, ... Similarly, the receiver portion **300** includes one or more latency paths **310**, **320**, ... Each of the latency paths in the transmitter portion **200** includes a framer, coder, and interleaver designated as **212**, **214**, **216** and **222**, **224** and **226**, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as **312**, **314**, **316** and **322**, **324**, and **326**, respectively. The transceiver **100** further includes a shared processing module **110**, a shared memory **120**, a parameter determination module **130**, a path module **140**, an allocation module **150**, and a shared resource management module **160**, all interconnected by one or more links (not shown).

In this exemplary embodiment, the transceiver **100** is illustrated with four total transmitter portion and receiver portion latency paths, i.e., **210**, **220**, **310**, and **320**. The shared memory **120** is shared amongst the two transmitter portion interleavers **216** and **226** and two receiver portion deinterleavers **316** and **326**. The shared processing module **110**, such as a shared coding module, is shared between the two transmitter portion coders **214** and **224** and the two receiver portion decoders **314** and **324**.

While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of

transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path **210**, the interleaver **216** could be allocated a portion of the shared memory **120**, while the coder **214** could be allocated to a dedicated processing module, vice versa, or the like.

In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory **120**, and a coding module, such as shared processing module **110**. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module **110**, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory **120** to an interleaver, such as interleaver **216** in the transmitter portion of the transceiver and allocate a second portion of the shared memory **120** to a deinterleaver, such as **316**, in the receiver portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory **120**, and be designed to allocate a first portion of shared memory **120** to a first interleaver, e.g., **216**, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., **226**, in the transmitter portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory **120** to a first deinterleaver, e.g., **316**, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., **326**, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory **120**.

Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module **140**, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module **130** then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module **150** allocates a portion of the shared memory **120** to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management **160**, the transceiver **100** transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require N*D=255*64=16 Kbytes of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

A second transmitter portion or receiver portion latency path may carry an internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). This latency path will require N*D=128*32=4 Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least (16+4)=20 Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with N=255/R=16 and N=128/R=8.

According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in

ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). Each latency path will require N*D=128*32=4 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with N=128/R=16, N=128/R=8 and N=128/R=8.

Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only 2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes (N=200) with 10 checkbytes (R=10) and interleaving/deinterleaving using an interleaver depth of 50 (D=50). Each latency path will require N*D=200*50=10 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

Number of supported transmitter and receiver latency paths=3
Max Interleaver Memory for latency path #1=16 Kbytes
Max Interleaver Memory for latency path #2=16 Kbytes
Max Interleaver Memory for latency path #3=16 Kbytes
Maximum total/shared memory for all latency paths=20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1—Video: N=255, R=16, D=64
latency path #2—Video: N=128, R=8, D=32
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would result in a total interleaver memory of 20 kbytes.

Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1—Video: N=200, R=10, D=50
latency path #2—Video: N=200, R=10, D=50
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would also result in a total interleaver memory of 20 kbytes.

Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

FIG. **2** outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step **S200** and continues to step **S210**. In step **S210**, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step **S220** where the control sequence ends.

FIG. **3** outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step **S310**. In step **S310**, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step **S320**, the determined maximum amount for one or more of the deinterleavers and/or interleavers is

transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S**330** where the control sequence ends.

FIG. **4** outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S**400** and continues to step S**410**. In step S**410**, the number of latency paths are determined Then, in step S**420**, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S**430**.

In step S**430**, and for each latency path, the steps in step **440** are performed.

In step S**440**, and while monitoring of allocation of resources is being performed, steps **450** and **460** are performed. More specifically, in step S**450**, one or more parameters associated with the communication system are determined. Then, in step S**460**, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S**470**.

In step S**470**, the allocation of shared resources is communicated to another transceiver. Next, in step S**480**, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S**410**. Otherwise, control jumps to step S**490** where the control sequence ends.

The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

The invention claimed is:

1. A system for allocating shared memory comprising:

means for transmitting or receiving, by a transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

means for determining, at the transceiver, an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

means for allocating, in the transceiver, a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

means for allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

means for interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

2. The system of claim **1**, wherein the determining is based on an impulse noise protection requirement.

3. The system of claim 1, wherein the determining is based on a latency requirement.

4. The system of claim 1, wherein the determining is based on a bit error rate requirement.

5. A system for allocating shared memory comprising:

means for transmitting or receiving, by a transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

means for determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

means for allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

means for allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

means for deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shred memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

6. The system of claim 5, wherein the determining is based on an impulse noise protection requirement.

7. The system of claim 5, wherein the determining is based on a latency requirement.

8. The system of claim 5, wherein the determining is based on a bit error rate requirement.

9. A system that allocates shared memory comprising:

a transceiver that performs:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

10. The system of claim 9 wherein the determining is based on an impulse noise protection requirement.

11. The system of claim 9, wherein the determining is based on a latency requirement.

12. The system of claim 9, wherein the determining is based on a bit error rate requirement.

13. A system that allocates shared memory comprising:

a transceiver that performs:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shred memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

14. The system of claim 13, wherein the determining is based on an impulse noise protection requirement.

15. The system of claim 13, wherein the determining is based on a latency requirement.

16. The system of claim 13, wherein the determining is based on a bit error rate requirement.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,844,882 B2
APPLICATION NO. : 12/761586
DATED : November 30, 2010
INVENTOR(S) : Marcos C. Tzannes et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

ln column 11, claim 5, line 17, delete “transmission” and insert -- reception --

ln column 11, claim 5, line 23, delete “received” and insert -- transmitted --

ln column 11, claim 5, line 28, delete “shred” and insert -- shared --

ln column 12, claim 13, line 29, delete “transmission” and insert -- reception --

ln column 12, claim 13, line 35, delete “received” and insert -- transmitted --

ln column 12, claim 13, line 40, delete “shred” and insert -- shared --

Signed and Sealed this
Third Day of May, 2011

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office

US008276048B2

(12) **United States Patent**
Tzannes et al.

(10) **Patent No.: US 8,276,048 B2**
(45) **Date of Patent: *Sep. 25, 2012**

(54) **RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT**

(75) Inventors: **Marcos C. Tzannes**, Orinda, CA (US); **Michael Lund**, West Newton, MA (US)

(73) Assignee: **Aware, Inc.**, Bedford, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **12/901,699**

(22) Filed: **Oct. 11, 2010**

(65) **Prior Publication Data**

US 2011/0029844 A1 Feb. 3, 2011

Related U.S. Application Data

(63) Continuation of application No. 12/761,586, filed on Apr. 16, 2010, now Pat. No. 7,844,882, which is a continuation of application No. 11/246,163, filed on Oct. 11, 2005, now Pat. No. 7,831,890.

(60) Provisional application No. 60/618,269, filed on Oct. 12, 2004.

(51) **Int. Cl.**

H03M 13/00	(2006.01)
H04B 1/38	(2006.01)
G06F 13/00	(2006.01)
G06F 15/16	(2006.01)

(52) **U.S. Cl.** **714/774**; 714/784; 375/222; 711/147; 711/157; 709/215

(58) **Field of Classification Search** 714/774, 714/784; 375/222; 711/147, 157; 709/215
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,524,116 A	6/1996	Kalmanek, Jr. et al.
5,663,910 A	9/1997	Ko et al.
6,098,188 A	8/2000	Kalmanek, Jr. et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP	1041756	10/2000

(Continued)

OTHER PUBLICATIONS

Notice of Allowance for Japanese Patent Application No. 2007-535818, dispatched Dec. 12, 2011.

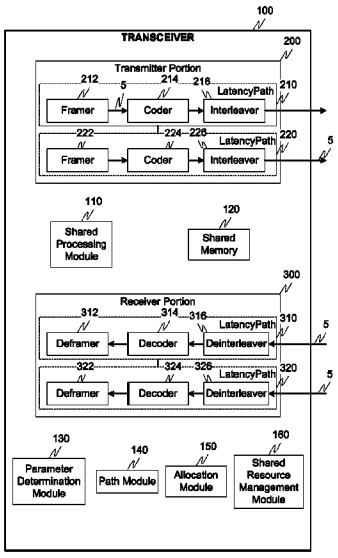
(Continued)

Primary Examiner — John J Tabone, Jr.
(74) *Attorney, Agent, or Firm* — Jason H. Vick; Sheridan Ross, PC

(57) **ABSTRACT**

A system allocates shared memory by transmitting/receiving a message specifying a maximum number of bytes of memory that are available to be allocated to an interleaver. The system determines an amount of memory required by the interleaver to interleave a first plurality of RS coded data bytes within a shared memory and allocates a first number of bytes of the shared memory to the interleaver to interleave the first plurality of RS coded data bytes for transmission at a first data rate. The system also allocates a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate and interleaves the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaves the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver.

8 Claims, 3 Drawing Sheets



U.S. PATENT DOCUMENTS

6,337,877	B1	1/2002	Cole et al.	
6,707,822	B1 *	3/2004	Fadavi-Ardekani et al.	370/395.5
6,775,320	B1 *	8/2004	Tzannes et al.	375/222
6,778,589	B1	8/2004	Ishii	
6,778,596	B1 *	8/2004	Tzannes	375/222
6,826,589	B2	11/2004	Berrada	
7,164,654	B2	1/2007	Hunzinger et al.	
7,200,792	B2	4/2007	Kim et al.	
7,519,124	B2 *	4/2009	Oksman et al.	375/260
7,657,818	B2 *	2/2010	Cioffi et al.	714/755
7,782,758	B2	8/2010	Wydrowski et al.	
7,831,890	B2 *	11/2010	Tzannes et al.	714/774
7,836,381	B1 *	11/2010	Tzannes et al.	714/774
7,844,882	B2 *	11/2010	Tzannes et al.	714/774
2001/0014962	A1	8/2001	Obuchi et al.	
2002/0154600	A1	10/2002	Ido et al.	
2003/0067877	A1	4/2003	Sivakumar et al.	
2004/0114536	A1	6/2004	O'Rourke	
2005/0180323	A1	8/2005	Beightol et al.	
2006/0088054	A1 *	4/2006	Tzannes et al.	370/468
2006/0236045	A1 *	10/2006	Keyes, Jr.	711/157
2009/0300450	A1	12/2009	Tzannes	
2010/0205501	A1	8/2010	Tzannes	
2010/0332935	A1	12/2010	Tzannes	
2011/0002331	A1 *	1/2011	Tzannes	370/389
2011/0029844	A1 *	2/2011	Tzannes et al.	714/774

FOREIGN PATENT DOCUMENTS

EP	1225735	7/2002
EP	1246409	10/2002
GB	2389493	12/2003
JP	06-164648	6/1994
JP	07-254862	10/1995
JP	2000-341247	12/2000
JP	2002-084338	3/2002
JP	2003-509966	3/2003
JP	2003-224615	8/2003
JP	2004-030506	1/2004
JP	2004-056221	2/2004
JP	2005-522963	7/2005
KR	10-2000-0047827	7/2000
WO	WO00/52834	9/2000
WO	WO 01/20865	3/2001
WO	WO 03/063060	7/2003
WO	WO 03/090011	10/2003
WO	WO 2006/044227	4/2006

OTHER PUBLICATIONS

Official Action (including translation) for Japanese Patent Application No. 2009-505623, dispatched Oct. 31, 2011.
Official Action (including translation) for Chinese Patent Application No. 200580032703, dispatched May 18, 2011.
Invitation to Pay Additional Fees (including partial international search report) for International (PCT) Patent Application No. PCT/US2007/066522, mailed Feb. 6, 2008.
International Search Report for International (PCT) Patent Application No. PCT/US2007/066522, mailed Apr. 14, 2008.
Written Opinion for International (PCT) Patent Application No. PCT/US2007/066522, mailed Apr. 14, 2008.
International Preliminary Report on Patentability for International (PCT) Patent Application No. PCT/US2007/066522, mailed Oct. 23, 2008.
Examiner's First Report on Australian Patent Application No. 2007257055, mailed Mar. 30, 2010.
Official Action (including translation) for Chinese Patent Application No. 200780012891.0, dispatched Mar. 16, 2011.
Official Action for Columbian Patent Application No. 08-109-377, dated Nov. 5, 2010.
Examination Report for European Patent Application No. 07811844.5, mailed Apr. 1, 2009.
Official Action for European Patent Application No. 07811844.5, dated Jul. 9, 2010.
Official Action for European Patent Application No. 07811844.5, dated Dec. 21, 2010.
European Search Report and Opinion for European Patent Application No. 10000017.3, dated Mar. 17, 2010.
Official Action for European Patent Application No. 10000017.3, dated Nov. 3, 2010.
European Search Report and Opinion for European Patent Application No. 10000016.5, dated Mar. 3, 2010.
Official Action for European Patent Application No. 10000016.5, dated Nov. 3, 2010.
Official Action for Japanese Patent Application No. 2009-505623, dispatched Apr. 4, 2011.
Official Action for Japanese Patent Application No. 2010-017356, dispatched Apr. 18, 2011.
Official Action (including translation) for Mexican Patent Application No. 27675, dated Apr. 22, 2010.
Official Action (translation only) for Korean Patent Application No. 10-2007-7008270, mailed Jun. 30, 2011.
Official Action (translation only) for Korean Patent Application No. 10-2007-7022463, mailed Jun. 30, 2011.
Official Action (including translation) for Japanese Patent Application No. 2007-535818, dispatched Jul. 11, 2011.
Official Action (including translation) for Japanese Patent Application No. 2010-017356, dispatched Aug. 29, 2011.
Official Action (including translation) for Mexican Patent Application No. 27675, dated Aug. 9, 2011.
Shoji, T. et al: "Wireless Access Method to Ensure Each Users QOS in Unpredictable and Various QOS Requirements Wireless Personal Communications," Springer, Dordrecht, NL, vol. 22, No. 2, Aug. 2002, pp. 139-151.
"ITU-T Recommendation G.992.5—Series G: Transmission Systems and Media, Digital Systems and Networks", International Telecommunication Union, ADSL2, May 2003, 92 pages.
"ITU-T Recommendation G.992.3," International Telecommunication Union, ADSL2, Jan. 2005, 436 pages.
"VDSL2 ITU-T Recommendation G.993.2," International Telecommunication Union, Feb. 2006, 252 pages.
"Sunset xDSL: Prequalification of ADSL Circuits with ATU-C Emulation," Sunrise Telecom Inc., Application Series, 2001, San Jose, USA, p. 3, available at http://www.sunrisetelecom.com/technotes/APP-xDSL-8B.pdf.
International Search Report for International (PCT) Patent Application No. PCT/US2005/036015, mailed Feb. 8, 2006.
Written Opinion for International (PCT) Patent Application No. PCT/US2005/036015, mailed Feb. 8, 2006.
International Preliminary Report on Patentability for International (PCT) Patent Application No. PCT/US2005/036015, mailed Apr. 26, 2007.
Examiner's First Report for Australian Patent Application No. 2005296086, mailed Jun. 24, 2009.
Notification of the First Office Action (including translation) for Chinese Patent Application No. 200580032703, mailed Sep. 25, 2009.
Official Action for U.S. Appl. No. 11/246,163, mailed Feb. 24, 2009.
Official Action for U.S. Appl. No. 11/246,163, mailed Dec. 9, 2009.
Notice of Allowability for U.S. Appl. No. 11/246,163, mailed Sep. 7, 2010.
Notice of Allowability for U.S. Appl. No. 12/761,586, mailed Oct. 6, 2010.
Notice of Allowability for U.S. Appl. No. 12/853,020, mailed Oct. 6, 2010.
Official Action (including translation) for Japanese Patent Application No. 2008-264540, dispatched Dec. 12, 2011.
Official Action for U.S. Appl. No. 12/295,828, mailed Jan. 5, 2012.
Official Notification of Intent to Grant (including translation) for Mexican Patent Application No. MX/a/2008/012505, mailed Apr. 3, 2012.
Notice of Allowance (including translation) for Korean Patent Application No. 10-2007-7008270, mailed Mar. 29, 2012.
Notice of Allowance (including translation) for Korean Patent Application No. 10-2010-7022463, mailed Mar. 29, 2012.
Notice of Allowance for Japanese Patent Application No. 2008-264540, mailed Mar. 26, 2012.

Notification of the Second Office Action (including translation) for Chinese Patent Application No. 200780012891.0, dispatched Mar. 7, 2012.
Official Action for U.S. Appl. No. 12/760,728, mailed Apr. 27, 2012.
Official Action for U.S. Appl. No. 12/783,765, mailed May 17, 2012.
Official Action (including translation) for Chinese Patent Application No. 200580032703.1, dispatched Mar. 28, 2012.
Decision of Final Rejection for Japanese Patent Application No. 2010-017356, dispatched Apr. 23, 2012.
Official Action for European Patent Application No. 10000016.5, dated Dec. 22, 2011.

* cited by examiner

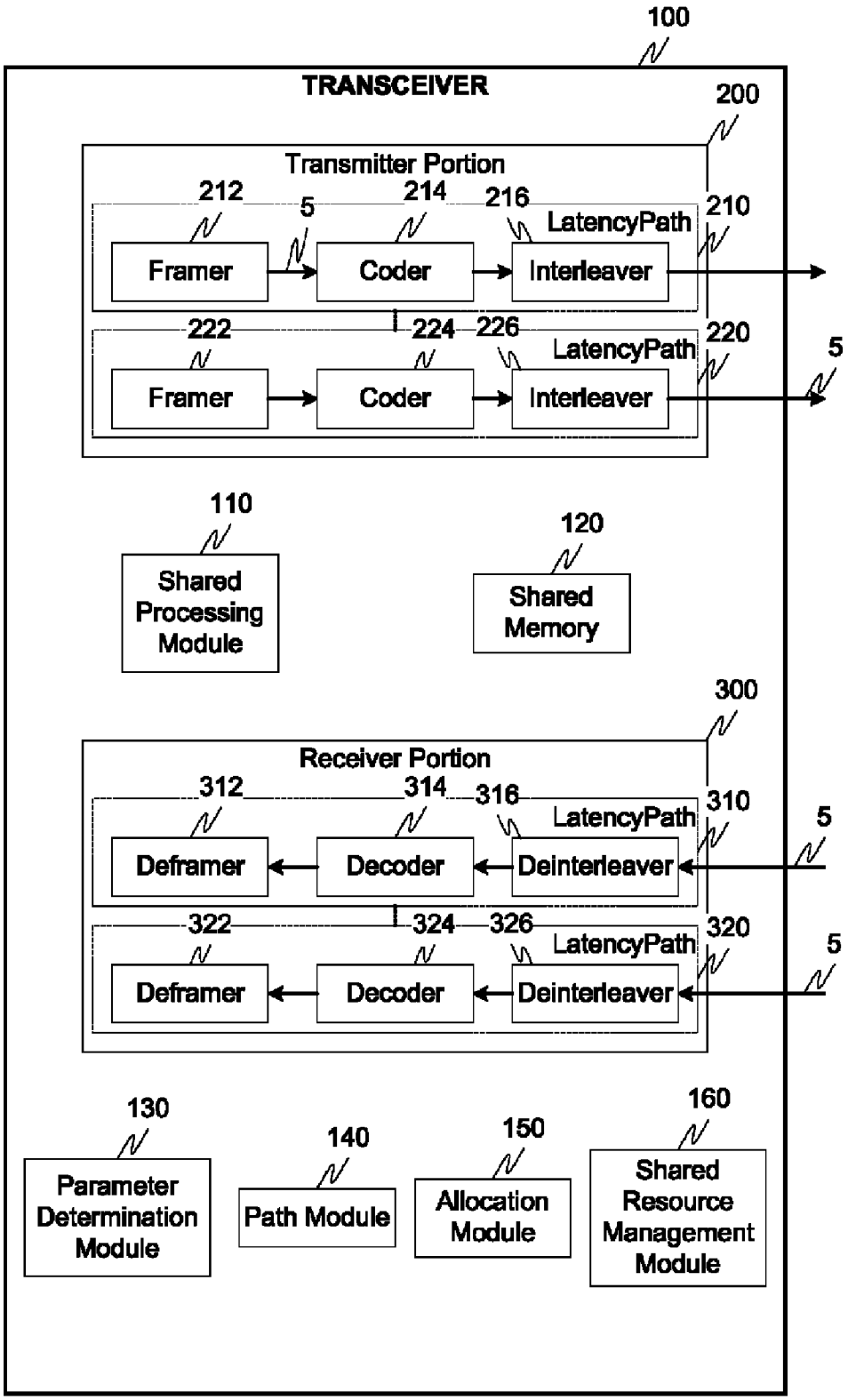

100
TRANSCEIVER
200
Transmitter Portion
212
5
214
216
LatencyPath
210
Framer
Coder
Interleaver
222
224
226
LatencyPath
220
5
Framer
Coder
Interleaver
110
Shared Processing Module
120
Shared Memory
300
Receiver Portion
312
314
316
LatencyPath
310
5
Deframer
Decoder
Deinterleaver
322
324
326
LatencyPath
320
5
Deframer
Decoder
Deinterleaver
130
Parameter Determination Module
140
Path Module
150
Allocation Module
160
Shared Resource Management Module

Fig. 1

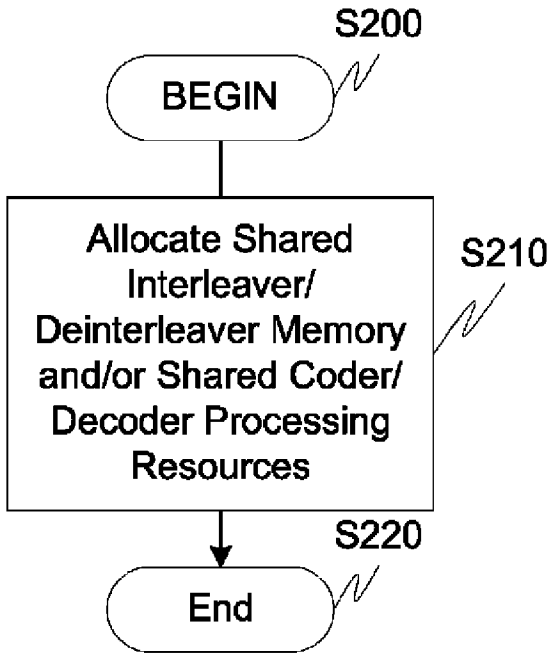

S200
BEGIN
Allocate Shared Interleaver/ Deinterleaver Memory and/or Shared Coder/ Decoder Processing Resources
S210
S220
End

Fig. 2

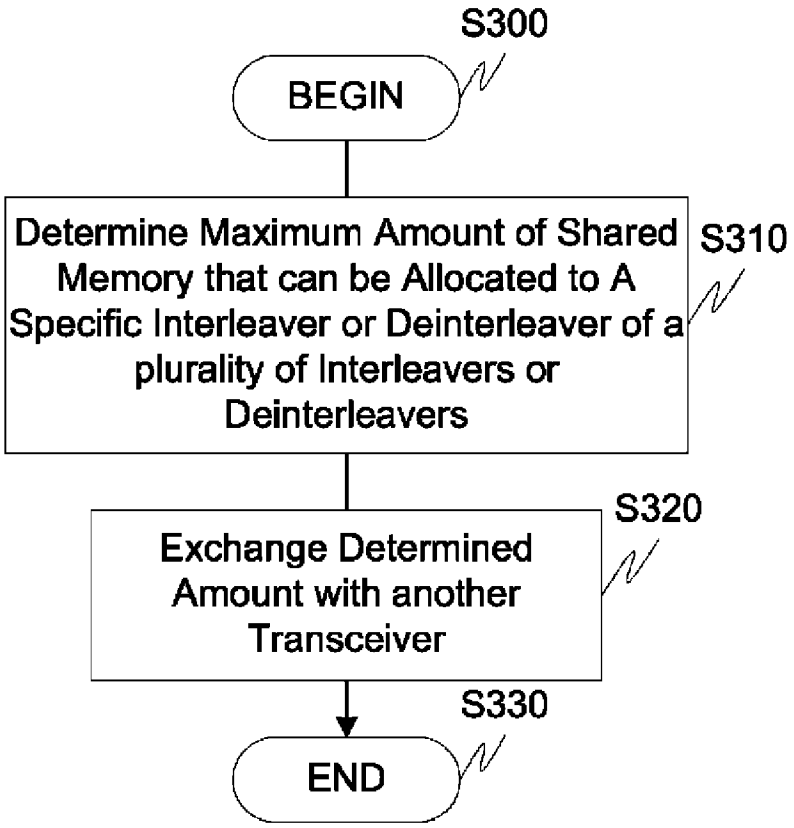

S300
BEGIN
Determine Maximum Amount of Shared Memory that can be Allocated to A Specific Interleaver or Deinterleaver of a plurality of Interleavers or Deinterleavers
S310
Exchange Determined Amount with another Transceiver
S320
S330
END

Fig. 3

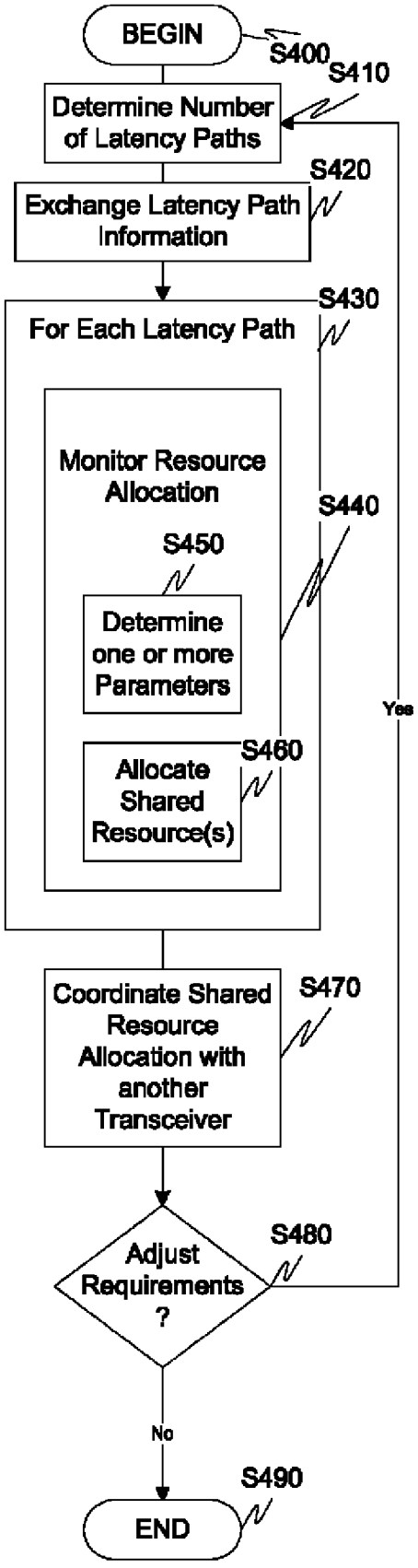

BEGIN
S400
S410
Determine Number of Latency Paths
S420
Exchange Latency Path Information
S430
For Each Latency Path
Monitor Resource Allocation
S440
S450
Determine one or more Parameters
S460
Allocate Shared Resource(s)
Yes
S470
Coordinate Shared Resource Allocation with another Transceiver
S480
Adjust Requirements ?
No
S490
END

Fig. 4

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

This application is a Continuation of U.S. application Ser. No. 12/761,586, filed Apr. 16, 2010, now U.S. Pat. No. 7,844,882, which is a Continuation of U.S. application Ser. No. 11/246,163 filed Oct. 11, 2005, now U.S. Pat. No. 7,831,890, which claims the benefit of and priority under 35 U.S.C. §119(e) to U.S. Patent Application No. 60/618,269, filed Oct. 12, 2004, entitled "Sharing Memory and Processing Resources in DSL Systems," each of which are incorporated herein by reference in their entirety.

BACKGROUND

1. Field of the Invention

This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

2. Description of Related Art

U.S. Pat. Nos. 6,775,320 and 6,778,596 describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

As described in U.S. Pat. No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a combination thereof and a shared memory designed to be allocated to a plurality of the modules.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

FIG. **1** is a functional block diagram illustrating an exemplary transceiver according to this invention;

FIG. **2** is a flowchart outlining an exemplary method of sharing resources according to this invention;

FIG. **3** is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

FIG. **4** is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

Furthermore, it should be appreciated that the various links, including communications channel **5**, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used interchangeably.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100** that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver **100** can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100**. The transceiver **100** includes a transmitter portion **200** and a receiver portion **300**. The transmitter portion **200** includes one or more latency paths **210**, **220**, ... Similarly, the receiver portion **300** includes one or more latency paths **310**, **320**, ... Each of the latency paths in the transmitter portion **200** includes a framer, coder, and interleaver designated as **212**, **214**, **216** and **222**, **224** and **226**, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as **312**, **314**, **316** and **322**, **324**, and **326**, respectively. The transceiver **100** further includes a shared processing module **110**, a shared memory **120**, a parameter determination module **130**, a path module **140**, an allocation module **150**, and a shared resource management module **160**, all interconnected by one or more links (not shown).

In this exemplary embodiment, the transceiver **100** is illustrated with four total transmitter portion and receiver portion latency paths, i.e., **210**, **220**, **310**, and **320**. The shared memory **120** is shared amongst the two transmitter portion interleavers **216** and **226** and two receiver portion deinterleavers **316** and **326**. The shared processing module **110**, such

as a shared coding module, is shared between the two transmitter portion coders **214** and **224** and the two receiver portion decoders **314** and **324**.

While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path **210**, the interleaver **216** could be allocated a portion of the shared memory **120**, while the coder **214** could be allocated to a dedicated processing module, vice versa, or the like.

In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory **120**, and a coding module, such as shared processing module **110**. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module **110**, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory **120** to an interleaver, such as interleaver **216** in the transmitter portion of the transceiver and allocate a second portion of the shared memory **120** to a deinterleaver, such as **316**, in the receiver portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory **120**, and be designed to allocate a first portion of shared memory **120** to a first interleaver, e.g., **216**, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., **226**, in the transmitter portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory **120** to a first deinterleaver, e.g., **316**, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., **326**, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory **120**.

Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module **140**, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module **130** then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module **150** allocates a portion of the shared memory **120** to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management **160**, the transceiver **100** transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

EXAMPLE #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require N*D=255*64=16 Kbytes of interleaver memory at the transmitter (or deinterleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

A second transmitter portion or receiver portion latency path may carry an internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). This latency path will require N*D=128*32=4 Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least (16+4)=20 Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with N=255/R=16 and N=128/R=8.

According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

EXAMPLE #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). Each latency path will require N*D=128*32=4 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with N=128/R=16, N=128/R=8 and N=128/R=8.

EXAMPLE #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only 2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes (N=200) with 10 checkbytes (R=10) and interleaving/deinterleaving using an interleaver depth of 50 (D=50). Each latency path will require N*D=200*50=10 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g,. N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

Number of supported transmitter and receiver latency paths=3
Max Interleaver Memory for latency path #1=16 Kbytes
Max Interleaver Memory for latency path #2=16 Kbytes
Max Interleaver Memory for latency path #3=16 Kbytes
Maximum total/shared memory for all latency paths=20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1—Video: N=255, R=16, D=64
latency path #2—Video: N=128, R=8, D=32
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would result in a total interleaver memory of 20 kbytes.

Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1—Video: N=200, R=10, D=50
latency path #2—Video: N=200, R=10, D=50
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would also result in a total interleaver memory of 20 kbytes.

Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

FIG. **2** outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step **S200** and continues to step **S210**. In step **S210**, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step **S220** where the control sequence ends.

FIG. **3** outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step **S310**. In step **S310**, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is deter-

mined. Next, in step S**320**, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S**330** where the control sequence ends.

FIG. **4** outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S**400** and continues to step S**410**. In step S**410**, the number of latency paths are determined Then, in step S**420**, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S**430**.

In step S**430**, and for each latency path, the steps in step **440** are performed.

In step S**440**, and while monitoring of allocation of resources is being performed, steps **450** and **460** are performed. More specifically, in step S**450**, one or more parameters associated with the communication system are determined. Then, in step S**460**, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S**470**.

In step S**470**, the allocation of shared resources is communicated to another transceiver. Next, in step S**480**, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S**410**. Otherwise, control jumps to step S**490** where the control sequence ends.

The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

The invention claimed is:

1. A system that allocates shared memory comprising:

a transceiver that is capable of:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;

allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

2. The system of claim **1**, wherein the determining is based on an impulse noise protection requirement.

3. The system of claim 1, wherein the determining is based on a latency requirement.

4. The system of claim 1, wherein the determining is based on a bit error rate requirement.

5. A system that allocates shared memory comprising:

a transceiver that is capable of:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;

allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

6. The system of claim 5, wherein the determining is based on an impulse noise protection requirement.

7. The system of claim 5, wherein the determining is based on a latency requirement.

8. The system of claim 5, wherein the determining is based on a bit error rate requirement.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 8,276,048 B2
APPLICATION NO. : 12/901699
DATED : September 25, 2012
INVENTOR(S) : Marcos C. Tzannes et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims:

At Column 11, Claim 5, line 16, delete "transmission" and insert -- reception --

At Column 12, Claim 5, line 3, delete "received" and insert -- transmitted --

Signed and Sealed this
Twenty-eighth Day of October, 2014

Michelle K. Lee

Michelle K. Lee
Deputy Director of the United States Patent and Trademark Office

US008495473B2

(12) **United States Patent**
Tzannes et al.

(10) **Patent No.: US 8,495,473 B2**
(45) **Date of Patent: Jul. 23, 2013**

(54) **RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT**

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(73) Assignee: **TQ Delta, LLC**, Austin, TX (US)

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(63) Continuation of application No. 12/901,699, filed on Oct. 11, 2010, now Pat. No. 8,276,048, which is a continuation of application No. 12/761,586, filed on Apr. 16, 2010, now Pat. No. 7,844,882, which is a continuation of application No. 11/246,163, filed on Oct. 11, 2005, now Pat. No. 7,831,890.

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(51) **Int. Cl.**

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G06F 13/00	(2006.01)
G06F 15/16	(2006.01)

(52) **U.S. Cl.**

USPC **714/774**; 714/784; 375/222; 711/147; 711/157; 709/215

(58) **Field of Classification Search**

USPC 714/774, 784; 375/222; 711/147, 711/157; 709/215

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,524,116	A	6/1996	Kalmanek, Jr. et al.
5,663,910	A	9/1997	Ko et al.
5,898,698	A	4/1999	Bross
5,983,382	A	11/1999	Pauls
6,098,188	A	8/2000	Kalmanek, Jr. et al.
6,337,877	B1	1/2002	Cole et al.
6,496,481	B1	12/2002	Wu et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP	1041756	10/2000
EP	1225735	7/2002

(Continued)

OTHER PUBLICATIONS

Notice of Allowance for U.S. Appl. No. 12/901,699, mailed Jul. 27, 2012.

(Continued)

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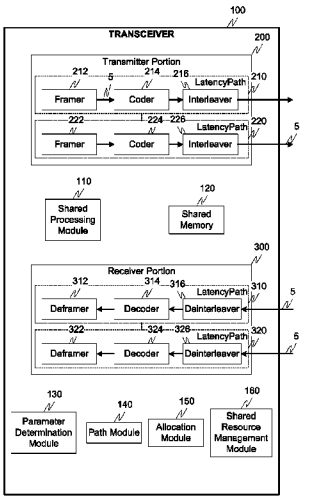
(74) *Attorney, Agent, or Firm* — Jason H. Vick; Sheridan Ross, PC

(57) **ABSTRACT**

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

46 Claims, 3 Drawing Sheets



U.S. PATENT DOCUMENTS

6,707,822	B1	3/2004	Fadavi-Ardekani et al.	
6,775,320	B1	8/2004	Tzannes et al.	
6,778,589	B1	8/2004	Ishii	
6,778,596	B1	8/2004	Tzannes	
6,826,589	B2	11/2004	Berrada	
7,164,654	B2	1/2007	Hunzinger et al.	
7,200,792	B2	4/2007	Kim et al.	
7,519,124	B2	4/2009	Oksman et al.	
7,600,172	B2	10/2009	Berens et al.	
7,657,818	B2	2/2010	Cioffi et al.	
7,764,595	B2	7/2010	Treigherman	
7,782,758	B2	8/2010	Wydrowski et al.	
7,831,890	B2	11/2010	Tzannes et al.	
7,836,381	B1	11/2010	Tzannes et al.	
7,844,882	B2	11/2010	Tzannes et al.	
8,149,904	B2 *	4/2012	Efland et al.	375/222
2001/0014962	A1	8/2001	Obuchi et al.	
2002/0087710	A1	7/2002	Aiken et al.	
2002/0154600	A1	10/2002	Ido et al.	
2003/0067877	A1	4/2003	Sivakumar et al.	
2003/0076870	A1	4/2003	Moon et al.	
2004/0114536	A1	6/2004	O'Rourke	
2004/0148552	A1	7/2004	Matsumoto et al.	
2005/0180323	A1	8/2005	Beightol et al.	
2006/0092871	A1	5/2006	Nishibayashi et al.	
2006/0236045	A1	10/2006	Keyes, Jr.	
2007/0263528	A1	11/2007	Mukherjee	
2009/0300450	A1	12/2009	Tzannes	
2010/0205501	A1	8/2010	Tzannes	
2010/0332935	A1	12/2010	Tzannes	
2011/0002331	A1	1/2011	Tzannes	
2011/0029844	A1	2/2011	Tzannes	

FOREIGN PATENT DOCUMENTS

EP	1246409	10/2002
GB	2389493	12/2003
JP	06-164648	6/1994
JP	07-254862	10/1995
JP	2000-341247	12/2000
JP	2002-084338	3/2002
JP	2003-509966	3/2003
JP	2003-224615	8/2003
JP	2004-030506	1/2004
JP	2004-056221	2/2004
JP	2005-522963	7/2005
KR	10-2000-0047827	7/2000
WO	WO00/52834	9/2000
WO	WO 01/20865	3/2001
WO	WO 03/063060	7/2003
WO	WO 03/090011	10/2003
WO	WO 2006/044227	4/2006

OTHER PUBLICATIONS

Notice of Allowance for U.S. Appl. No. 12/295,828, mailed Aug. 17, 2012.

Shoji, T. et al: "Wireless Access Method to Ensure Each Users QOS in Unpredictable and Various QOS Requirements Wireless Personal Communications," Springer, Dordrecht, NL, vol. 22, No. 2, Aug. 2002, pp. 139-151.

"ITU-T Recommendation G.992.5—Series G: Transmission Systems and Media, Digital Systems and Networks", International Telecommunication Union, ADSL2, May 2003, 92 pages.

"ITU-T Recommendation G.992.3," International Telecommunication Union, ADSL2, Jan. 2005, 436 pages.

"VDSL2 ITU-T Recommendation G.993.2," International Telecommunication Union, Feb. 2006, 252 pages.

"Sunset xDSL: Prequalification of ADSL Circuits with ATU-C Emulation," Sunrise Telecom Inc., Application Series, 2001, San Jose, USA, p. 3, available at http://www.sunrisetelecom.com/technotes/APP-xDSL-8B.pdf.

International Search Report for International (PCT) Patent Application No. PCT/US2005/036015, mailed Feb. 8, 2006.

Written Opinion for International (PCT) Patent Application No. PCT/US2005/036015, mailed Feb. 8, 2006.

International Preliminary Report on Patentability for International (PCT) Patent Application No. PCT/US2005/036015, mailed Apr. 26, 2007.

Examiner's First Report for Australian Patent Application No. 2005296086, mailed Jun. 24, 2009.

Notification of the First Office Action (including translation) for Chinese Patent Application No. 200580032703, mailed Sep. 25, 2009.

Official Action (including translation) for Chinese Patent Application No. 200580032703, dispatched May 18, 2011.

Official Action (including translation) for Chinese Patent Application No. 200580032703.1, dispatched Mar. 28, 2012.

Official Action (translation only) for Korean Patent Application No. 10-2007-7008270, mailed Jun. 30, 2011.

Notice of Allowance (including translation) for Korean Patent Application No. 10-2007-7008270, mailed Mar. 29, 2012.

Official Action (translation only) for Korean Patent Application No. 10-2010-7022463, mailed Jun. 30, 2011.

Notice of Allowance (including translation) for Korean Patent Application No. 10-2010-7022463, mailed Mar. 29, 2012.

Official Action (including translation) for Japanese Patent Application No. 2007-535818, dispatched Jul. 11, 2011.

Notice of Allowance for Japanese Patent Application No. 2007-535818, dispatched Dec. 12, 2011.

Official Action (including translation) for Japanese Patent Application No. 2008-264540, dispatched Jul. 11, 2011.

Official Action (including translation) for Japanese Patent Application No. 2008-264540, dispatched Dec. 12, 2011.

Notice of Allowance for Japanese Patent Application No. 2008-264540, mailed Mar. 26, 2012.

Invitation to Pay Additional Fees (including partial international search report) for International (PCT) Patent Application No. PCT/US2007/066522, mailed Feb. 6, 2008.

International Search Report for International (PCT) Patent Application No. PCT/US2007/066522, mailed Apr. 14, 2008.

Written Opinion for International (PCT) Patent Application No. PCT/US2007/066522, mailed Apr. 14, 2008.

International Preliminary Report on Patentability for International (PCT) Patent Application No. PCT/US2007/066522, mailed Oct. 23, 2008.

Examiner's First Report on Australian Patent Application No. 2007257055, mailed Mar. 30, 2010.

Official Action (including translation) for Chinese Patent Application No. 200780012891.0, dispatched Mar. 16, 2011.

Notification of the Second Office Action (including translation) for Chinese Patent Application No. 200780012891.0, dispatched Mar. 7, 2012.

Official Action for Columbian Patent Application No. 08-109-377, dated Nov. 5, 2010.

Examination Report for European Patent Application No. 07811844.5, mailed Apr. 1, 2009.

Official Action for European Patent Application No. 07811844.5, dated Jul. 9, 2010.

Official Action for European Patent Application No. 07811844.5, dated Dec. 21, 2010.

European Search Report and Opinion for European Patent Application No. 10000017.3, dated Mar. 17, 2010.

Official Action for European Patent Application No. 10000017.3, dated Nov. 3, 2010.

European Search Report and Opinion for European Patent Application No. 10000016.5, dated Mar. 3, 2010.

Official Action for European Patent Application No. 10000016.5, dated Nov. 3, 2010.

Official Action for European Patent Application No. 10000016.5, dated Dec. 22, 2011.

Official Action for Japanese Patent Application No. 2009-505623, dispatched Apr. 4, 2011.

Official Action (including translation) for Japanese Patent Application No. 2009-505623, dispatched Oct. 31, 2011.

Official Action for Japanese Patent Application No. 2010-017356, dispatched Apr. 18, 2011.

Official Action (including translation) for Japanese Patent Application No. 2010-017356, dispatched Aug. 29, 2011.

Decision of Final Rejection for Japanese Patent Application No. 2010-017356, dispatched Apr. 23, 2012.
Official Action (including translation) for Mexican Patent Application No. MX/a/2008/012505, dated Apr. 22, 2010.
Official Action (including translation) for Mexican Patent Application No. MX/a/2008/012505, dated Aug. 9, 2011.
Official Notification of Intent to Grant (including translation) for Mexican Patent Application No. MX/a/2008/012505, mailed Apr. 3, 2012.
Official Action for U.S. Appl. No. 11/246,163, mailed Feb. 24, 2009.
Official Action for U.S. Appl. No. 11/246,163, mailed Dec. 9, 2009.
Notice of Allowability for U.S. Appl. No. 11/246,163, mailed Sep. 7, 2010.
Notice of Allowability for U.S. Appl. No. 12/761,586, mailed Oct. 6, 2010.
Notice of Allowability for U.S. Appl. No. 12/853,020, mailed Oct. 6, 2010.
Official Action for U.S. Appl. No. 12/901,699, mailed Jan. 6, 2012.
Official Action for U.S. Appl. No. 12/295,828, mailed Jan. 5, 2012.
Official Action for U.S. Appl. No. 12/760,728, mailed Apr. 27, 2012.
Official Action for U.S. Appl. No. 12/783,765, mailed May 17, 2012.
Official Action for European Application No. 05807443.6, mailed Mar. 6, 2013.
Official Action for European Patent Application No. 07811844,5, dated Dec. 18, 2012.
Communication Under Rule 71(3) EPC—Intention to Grant for European Patent Application No. 10000016.5, dated Dec. 18, 2012.
Examiner's Report for Canadian Patent Application No. 2,580,280, mailed Sep. 14, 2012.
Decision of Refusal (including translation) for Chinese Patent Application No. 200580032703.1, dispatched Sep. 5, 2012.
U.S. Appl. No. 13/766,059, filed Feb. 13, 2013, Tzannes.
Notification of the Second Office Action (including translation) for Chinese Patent Application No. 200780012891.0, dispatched Dec. 12, 2012.
Notice of Allowance for U.S. Appl. No. 12/783,758, mailed Dec. 26, 2012.
Official Action for U.S. Appl. No. 12/760,728, mailed Jan. 2, 2013.
Official Action for U.S. Appl. No. 12/783,765, mailed Dec. 17, 2012.
Examiner's First Report for Australian Patent Application No. 2011201250 mailed May 13, 2013.
First Examination Report for Indian Patent Application No. 1208/KOLNP/2007, mailed Mar. 18, 2013.
Notice of Allowance for U.S. Appl. No. 12/783,765, mailed May 9, 2013.

* cited by examiner

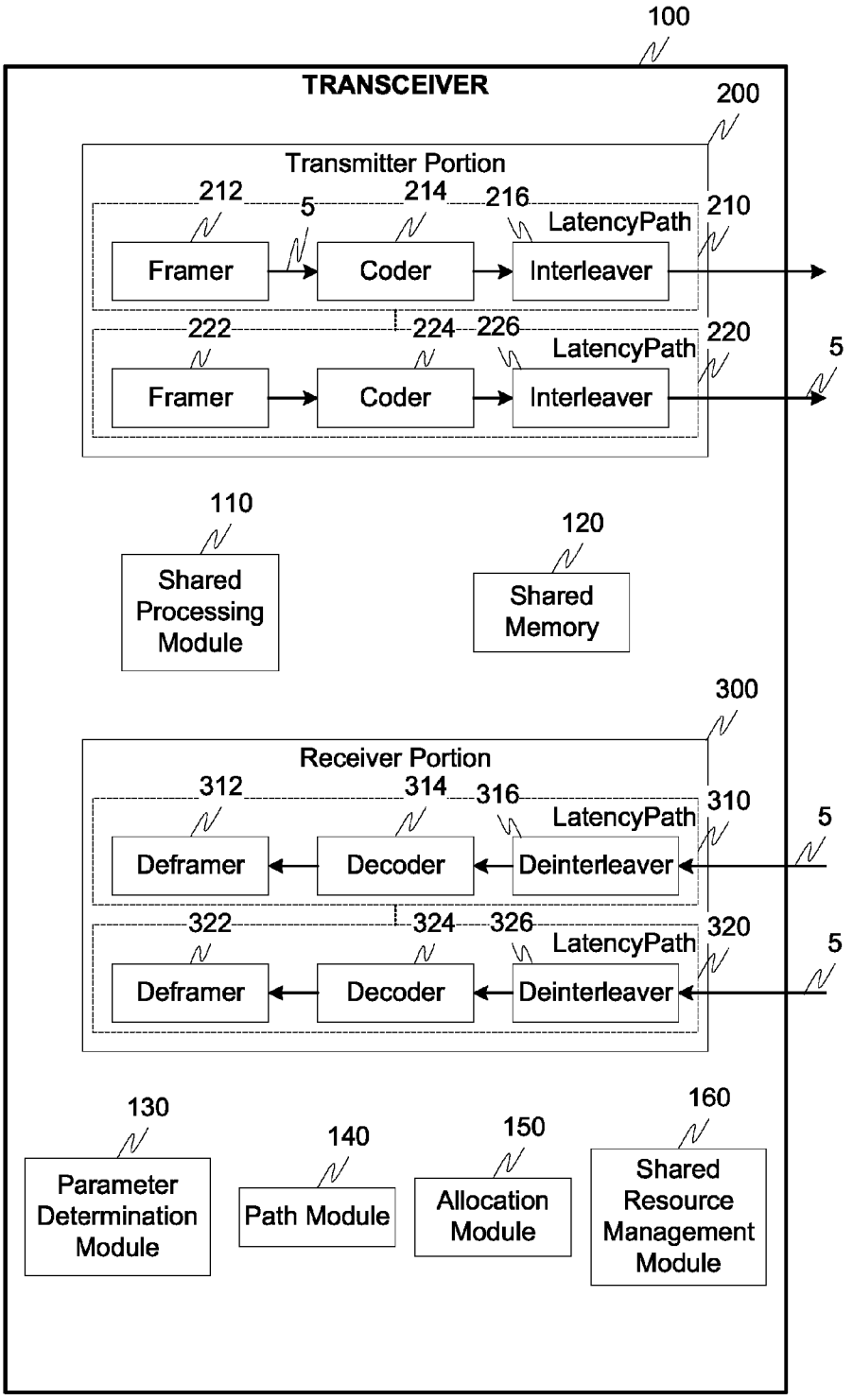

100
TRANSCEIVER
200
Transmitter Portion
212
5
214
216
210
LatencyPath
Framer
Coder
Interleaver
222
224
226
220
LatencyPath
5
Framer
Coder
Interleaver
110
Shared Processing Module
120
Shared Memory
300
Receiver Portion
312
314
316
310
LatencyPath
5
Deframer
Decoder
Deinterleaver
322
324
326
320
LatencyPath
5
Deframer
Decoder
Deinterleaver
130
Parameter Determination Module
140
Path Module
150
Allocation Module
160
Shared Resource Management Module

Fig. 1

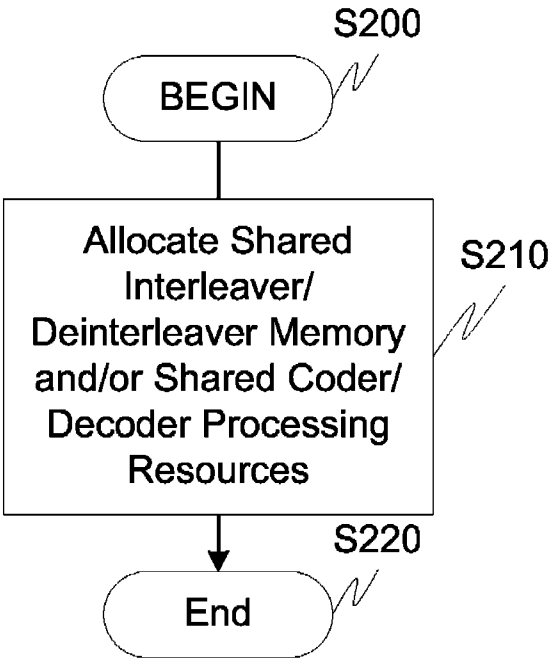

S200
BEGIN
Allocate Shared Interleaver/ Deinterleaver Memory and/or Shared Coder/ Decoder Processing Resources
S210
S220
End

Fig. 2

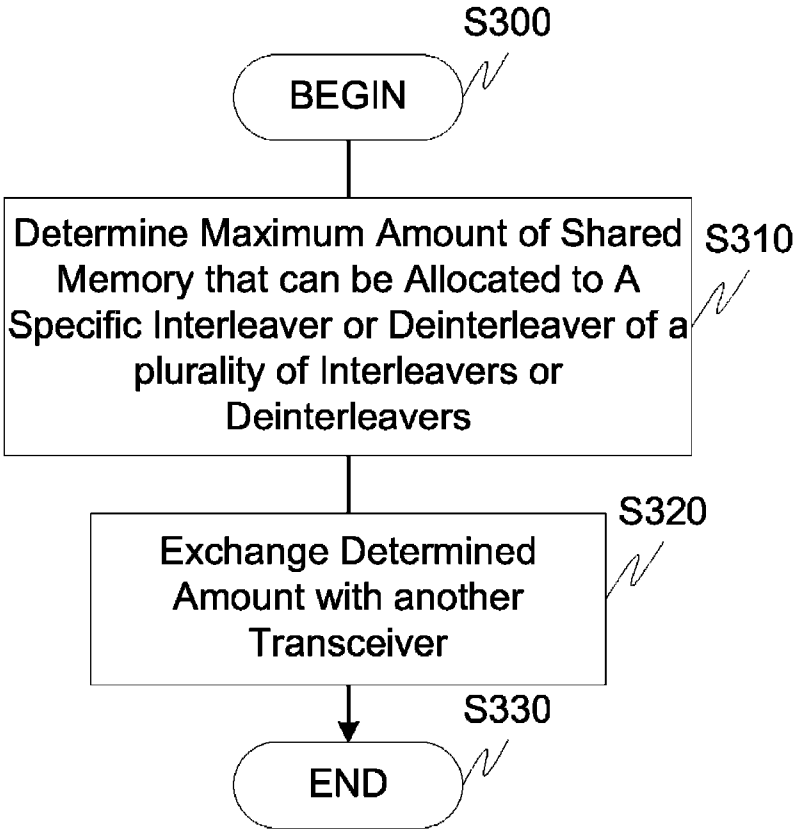

S300
BEGIN
Determine Maximum Amount of Shared Memory that can be Allocated to A Specific Interleaver or Deinterleaver of a plurality of Interleavers or Deinterleavers
S310
Exchange Determined Amount with another Transceiver
S320
S330
END

Fig. 3

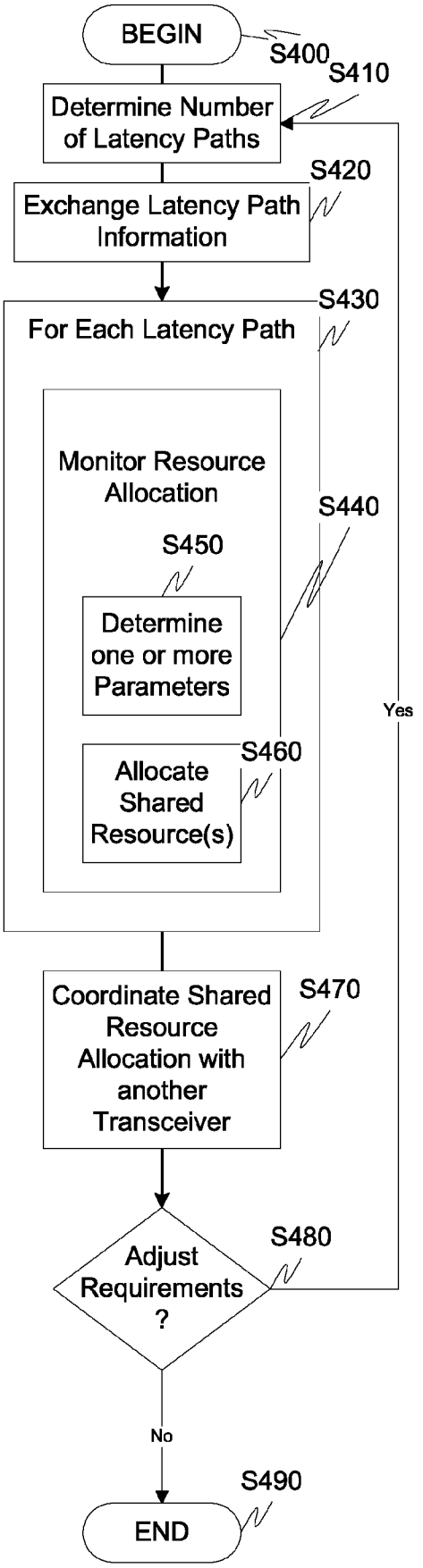

BEGIN
S400
S410
Determine Number of Latency Paths
S420
Exchange Latency Path Information
S430
For Each Latency Path
Monitor Resource Allocation
S440
S450
Determine one or more Parameters
S460
Allocate Shared Resource(s)
Yes
S470
Coordinate Shared Resource Allocation with another Transceiver
S480
Adjust Requirements ?
No
S490
END

Fig. 4

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

This application is a Continuation of U.S. application Ser. No. 12/901,699, filed Oct. 11, 2010, now U.S. Pat. No. 8,276,048, which is a Continuation of Ser. No. 12/761,586, filed Apr. 16, 2010, now U.S. Pat. No. 7,844,882, which is a Continuation of U.S. application Ser. No. 11/246,163 filed Oct. 11, 2005, now U.S. Pat. No. 7,831,890, which claims the benefit of and priority under 35 U.S.C. §119(e) to U.S. Patent Application No. 60/618,269, filed Oct. 12, 2004, entitled "Sharing Memory and Processing Resources in DSL Systems," each of which are incorporated herein by reference in their entirety.

BACKGROUND

1. Field of the Invention

This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

2. Description of Related Art

U.S. Pat. Nos. 6,775,320 and 6,778,596 describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

As described in U.S. Pat. No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

Additional aspects of this invention relate to configuring and initializing shared memory in a communication system.

More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a combination thereof and a shared memory designed to be allocated to a plurality of the modules.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

FIG. **1** is a functional block diagram illustrating an exemplary transceiver according to this invention;

FIG. **2** is a flowchart outlining an exemplary method of sharing resources according to this invention;

FIG. **3** is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

FIG. **4** is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used interchangeably.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100** that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver **100** can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100**. The transceiver **100** includes a transmitter portion **200** and a receiver portion **300**. The transmitter portion **200** includes one or more latency paths **210**, **220**, ... Similarly, the receiver portion **300** includes one or more latency paths **310**, **320**, ... Each of the latency paths in the transmitter portion **200** includes a framer, coder, and interleaver designated as **212**, **214**, **216** and **222**, **224** and **226**, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as **312**, **314**, **316** and **322**, **324**, and **326**, respectively. The transceiver **100** further includes a shared processing module **110**, a shared memory **120**, a parameter determination module **130**, a path module **140**, an allocation module **150**, and a shared resource management module **160**, all interconnected by one or more links (not shown).

In this exemplary embodiment, the transceiver **100** is illustrated with four total transmitter portion and receiver portion latency paths, i.e., **210**, **220**, **310**, and **320**. The shared memory **120** is shared amongst the two transmitter portion interleavers **216** and **226** and two receiver portion deinterleavers **316** and **326**. The shared processing module **110**, such

as a shared coding module, is shared between the two transmitter portion coders **214** and **224** and the two receiver portion decoders **314** and **324**.

While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path **210**, the interleaver **216** could be allocated a portion of the shared memory **120**, while the coder **214** could be allocated to a dedicated processing module, vice versa, or the like.

In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory **120**, and a coding module, such as shared processing module **110**. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module **110**, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory **120** to an interleaver, such as interleaver **216** in the transmitter portion of the transceiver and allocate a second portion of the shared memory **120** to a deinterleaver, such as **316**, in the receiver portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory **120**, and be designed to allocate a first portion of shared memory **120** to a first interleaver, e.g., **216**, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., **226**, in the transmitter portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory **120** to a first deinterleaver, e.g., **316**, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., **326**, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory **120**.

Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module **140**, the number of transmitter and receiver latency paths (N) is determined The parameter determination module **130** then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module **150** allocates a portion of the shared memory **120** to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management **160**, the transceiver **100** transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require N*D=255*64=16 Kbytes of interleaver memory at the transmitter (or deinterleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

A second transmitter portion or receiver portion latency path may carry an internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 1 (D=32). This latency path will require N*D=128*32=4 Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least (16+4)=20 Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with N=255/R=16 and N=128/R=8.

According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). Each latency path will require N*D=128*32=4 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with N=128/R=16, N=128/R=8 and N=128/R=8.

Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only 2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes (N=200) with 10 checkbytes (R=10) and interleaving/deinterleaving using an interleaver depth of 50 (D=50). Each latency path will require N*D=200*50=10 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

- Number of supported transmitter and receiver latency paths=3
- Max Interleaver Memory for latency path #1=16 Kbytes
- Max Interleaver Memory for latency path #2=16 Kbytes
- Max Interleaver Memory for latency path #3=16 Kbytes
- Maximum total/shared memory for all latency paths=20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1—Video: N=255, R=16, D=64
latency path #2—Video: N=128, R=8, D=32
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would result in a total interleaver memory of 20 kbytes.

Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1—Video: N=200, R=10, D=50
latency path #2—Video: N=200, R=10, D=50
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would also result in a total interleaver memory of 20 kbytes.

Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

FIG. **2** outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step S**200** and continues to step S**210**. In step S**210**, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S**220** where the control sequence ends.

FIG. **3** outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S**310**. In step S**310**, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is deter-

mined Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S330 where the control sequence ends.

FIG. 4 outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S400 and continues to step S410. In step S410, the number of latency paths are determined Then, in step S420, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S430.

In step S430, and for each latency path, the steps in step 440 are performed.

In step S440, and while monitoring of allocation of resources is being performed, steps 450 and 460 are performed. More specifically, in step S450, one or more parameters associated with the communication system are determined Then, in step S460, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S470.

In step S470, the allocation of shared resources is communicated to another transceiver. Next, in step S480, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S410. Otherwise, control jumps to step S490 where the control sequence ends.

The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

The invention claimed is:

1. A method for sharing resources in a multicarrier transceiver comprising:

sharing, in the transceiver, memory between an interleaver in a first latency path and a deinterleaver in a second latency path; and

transmitting or receiving, during initialization of the transceiver, a message, the message indicating how the shared memory is to be allocated to the interleaver in the first latency path or how the shared memory is to be allocated to the deinterleaver in the second latency path.

2. The method of claim 1, wherein the transceiver is connected to a second transceiver using a wired or wireless channel and the transceivers are used to transport video, internet access and voice data.

3. The method of claim 1, wherein the method is performed in a linecard that is capable of transporting video.

4. The method of claim 1, wherein the method is performed in a customer premises modem that is capable of transporting video.

5. The method of claim 1, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

6. The method of claim 1, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

7. The method of claim 6, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

8. The method of claim 1, wherein the transceiver includes at least one digital signal processor.

9. The method of claim 1, wherein the transceiver includes at least one ASIC.

10. A multicarrier communications transceiver with a shared memory, the transceiver capable of:

sharing the memory between an interleaver in a first latency path and

a deinterleaver in a second latency path; and

transmitting or receiving, during initialization of the transceiver, a message indicating how the shared memory is to be used by the interleaver or the deinterleaver.

11. The transceiver of claim 10, further comprising:

an allocation module designed to allocate the shared memory based on one or more communication parameters.

12. The transceiver of claim 11, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate (BER).

13. The transceiver of claim 10, wherein the transceiver is connected to a second transceiver using a wired or wireless channel and the transceivers are used to transport video, internet access and voice data.

14. The transceiver of claim 10, wherein the transceiver is located in a linecard that is capable of transporting video.

15. The transceiver of claim 10, wherein the transceiver is located in a customer premises modem that is capable of transporting video.

16. The transceiver of claim 10, further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules.

17. The transceiver of claim 10, wherein the transceiver includes at least one digital signal processor.

18. The transceiver of claim 10, wherein the transceiver includes at least one ASIC.

19. An apparatus comprising:

a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path, the multicarrier communications transceiver being associated with a memory,

wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver and wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

20. The apparatus of claim 19, wherein the message is based on one or more communication parameters.

21. The apparatus of claim 20, wherein at least one of the communication parameters is a data rate, a latency, an INP value, or a Bit Error Rate (BER).

22. The apparatus of claim 19, wherein the transceiver is configured to transport video, internet access and voice data using a wired or wireless channel.

23. The apparatus of claim 19, wherein the apparatus is a customer premises modem that is capable of transporting video.

24. The apparatus of claim 19, wherein the transceiver includes a shared processing module configured to provide processing resources to a plurality of coding and/or decoding modules.

25. The apparatus of claim 19, wherein the transceiver includes at least one digital signal processor.

26. The apparatus of claim 19, wherein the transceiver includes at least one ASIC.

27. The apparatus of claim 19, wherein a sum of a maximum amount of the memory that can be allocated to the interleaving function and a maximum amount of the memory that can be allocated to the deinterleaving function is more than a total amount of the memory.

28. An apparatus comprising:

a multicarrier communications transceiver that is configured to generate a message during an initialization of the transceiver, perform an interleaving function associated with a first latency path, and perform a deinterleaving function associated with a second latency path, the transceiver being associated with a memory,

wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time and wherein the generated message indicates how the memory has been allocated between the interleaving function and the deinterleaving function.

29. The apparatus of claim 28, wherein the message is based on one or more communication parameters.

30. The apparatus of claim 29, wherein at least one of the communication parameters is a data rate, a latency, an INP value, or a Bit Error Rate (BER).

31. The apparatus of claim 28, wherein the transceiver is configured to transport video, internet access and voice data using a wired or wireless channel.

32. The apparatus of claim 28, wherein the apparatus is a linecard that is capable of transporting video.

33. The apparatus of claim 28, wherein the transceiver includes a shared processing module configured to provide processing resources to a plurality of coding and/or decoding modules.

34. The apparatus of claim 28, wherein the transceiver includes at least one digital signal processor.

35. The apparatus of claim 28, wherein the transceiver includes at least one ASIC.

36. The apparatus of claim 28, wherein a sum of a maximum amount of the memory that can be allocated to the interleaving function and a maximum amount of the memory that can be allocated to the deinterleaving function is more than a total amount of the memory.

37. A method of operating components of a telecommunications network, the components including a first multicarrier communications transceiver located in a linecard and a second multicarrier communications transceiver located at a customer premises, the first transceiver being configured to perform a first interleaving function associated with a first latency path and perform a first deinterleaving function associated with a second latency path, the second transceiver being configured to perform a second deinterleaving function associated with the first latency path and perform a second interleaving function associated with the second latency path and each of the first and second transceivers being associated with a respective memory, the method comprising:

causing the first transceiver to allocate the memory associated with the first transceiver between the first interleaving function performed by the first transceiver and the first deinterleaving function performed by the first transceiver, wherein at least a portion of the memory associated with the first transceiver may be allocated to the first interleaving function performed by the first

transceiver or the first deinterleaving function performed by the first transceiver at any one particular time; and

causing the first transceiver to transmit a message to the second transceiver during an initialization of the second transceiver, wherein the message indicates how the memory associated with the second transceiver is to be allocated between the second interleaving function performed by the second transceiver and the second deinterleaving function performed by the second transceiver and wherein at least a portion of the memory associated with the second transceiver may be allocated to the second interleaving function performed by the second transceiver or the second deinterleaving function performed by the second transceiver at any one particular time depending on the message.

38. The method of claim **37**, wherein the message is transmitted or received using a wired or wireless channel and wherein the method further comprises causing the first transceiver to transport video, internet access and voice data using the wired or wireless channel.

39. The method of claim **37**, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules within the first transceiver.

40. The method of claim **37**, wherein the message is based on one or more communication parameters.

41. The method of claim **40**, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

42. The method of claim **37**, wherein the telecommunications network is a DSL network.

43. The method of claim **37**, wherein the first transceiver is included within a line card.

44. The method of claim **37**, wherein the second transceiver is included within a customer premises modem.

45. The method of claim **37**, wherein a sum of a maximum amount of the memory associated with the first transceiver that can be allocated to the first interleaving function performed by the first transceiver and a maximum amount of the memory associated with the first transceiver that can be allocated to the deinterleaving function performed by the first transceiver is more than a total amount of the memory associated with the first transceiver.

46. The method of claim **37**, wherein a sum of a maximum amount of the memory associated with the second transceiver that can be allocated to the second interleaving function performed by the second transceiver and a maximum amount of the memory associated with the second transceiver that can be allocated to the deinterleaving function performed by the second transceiver is more than a total amount of the memory associated with the second transceiver.

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(54) **RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT**

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(56) **References Cited**

U.S. PATENT DOCUMENTS

5,524,116	A	6/1996	Kalmanek, Jr. et al.
5,663,910	A	9/1997	Ko et al.
5,898,698	A	4/1999	Bross
5,983,382	A	11/1999	Pauls
6,098,188	A	8/2000	Kalmanek, Jr. et al.
6,337,877	B1	1/2002	Cole et al.
6,496,481	B1	12/2002	Wu et al.
6,707,822	B1	3/2004	Fadavi-Ardekani et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP	1041756	10/2000
EP	1225735	7/2002

(Continued)

OTHER PUBLICATIONS

Official Action for Korean Patent Application No. 10-2008-7024792, mailed Aug. 29, 2013.

(Continued)

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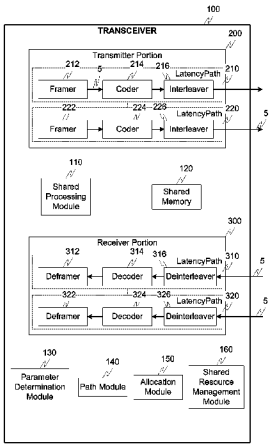
(74) *Attorney, Agent, or Firm* — Jason H. Vick; Sheridan Ross, PC

(57) **ABSTRACT**

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

28 Claims, 3 Drawing Sheets



(56) **References Cited**

U.S. PATENT DOCUMENTS

6,775,320	B1	8/2004	Tzannes et al.	
6,778,589	B1	8/2004	Ishii	
6,778,596	B1	8/2004	Tzannes	
6,826,589	B2	11/2004	Berrada	
7,164,654	B2	1/2007	Hunzinger et al.	
7,174,493	B2	2/2007	Matsumoto et al.	
7,200,792	B2	4/2007	Kim et al.	
7,519,124	B2	4/2009	Oksman et al.	
7,600,172	B2	10/2009	Berens et al.	
7,657,818	B2	2/2010	Cioffi et al.	
7,764,595	B2	7/2010	Treigherman	
7,782,758	B2	8/2010	Wydrowski et al.	
7,831,890	B2	11/2010	Tzannes et al.	
7,836,381	B1	11/2010	Tzannes et al.	
7,844,882	B2	11/2010	Tzannes et al.	
8,074,138	B2	12/2011	Chae et al.	
8,149,904	B2 *	4/2012	Efland et al.	375/222
8,276,048	B2	9/2012	Tzannes et al.	
8,335,956	B2	12/2012	Tzannes	
8,407,546	B2	3/2013	Tzannes	
8,468,411	B2	6/2013	Tzannes	
8,495,473	B2	7/2013	Tzannes et al.	
2001/0014962	A1	8/2001	Obuchi et al.	
2002/0087710	A1	7/2002	Aiken et al.	
2002/0154600	A1	10/2002	Ido et al.	
2003/0067877	A1	4/2003	Sivakumar et al.	
2003/0076870	A1	4/2003	Moon et al.	
2004/0114536	A1	6/2004	O'Rourke	
2004/0148552	A1	7/2004	Matsumoto et al.	
2004/0203455	A1	10/2004	Bao et al.	
2005/0180323	A1	8/2005	Beightol et al.	
2006/0092871	A1	5/2006	Nishibayashi et al.	
2006/0236045	A1	10/2006	Keyes, Jr.	
2007/0198898	A1	8/2007	Ysebaert et al.	
2007/0263528	A1	11/2007	Mukherjee	
2008/0212582	A1	9/2008	Zwart et al.	
2010/0061376	A1	3/2010	Shimizu	
2010/0205501	A1	8/2010	Tzannes	
2013/0163592	A1	6/2013	Tzannes	

FOREIGN PATENT DOCUMENTS

EP	1246409	10/2002
EP	1271833	1/2003
EP	1367809	1/2006
GB	2389493	12/2003
JP	06-164648	6/1994
JP	07-254862	10/1995
JP	Hei09-247048	9/1997
JP	Hei11-1507644	6/1999
JP	Hei11-355254 A	12/1999
JP	2000-341247	12/2000
JP	2002-084338	3/2002
JP	2003-008553	1/2003
JP	2003-509966	3/2003
JP	2003-224615	8/2003
JP	2004-007269	1/2004
JP	2004-030506	1/2004
JP	2004-056221	2/2004
JP	2004-135013	4/2004
JP	2005-522963	7/2005
JP	2005-526422	9/2005
KR	10-2000-0047827	7/2000
WO	WO 00/52834	9/2000
WO	WO 01/20865	3/2001
WO	WO 03/028296	4/2003
WO	WO 03/063060	7/2003
WO	WO 03/090011	10/2003

OTHER PUBLICATIONS

Official Action (including translation) for Mexican Patent Application No. MX/a/2011/005751, dated Jun. 6, 2013.

Shoji, T. et al: "Wireless Access Method to Ensure Each Users QOS in Unpredictable and Various QOS Requirements Wireless Personal Communications," Springer, Dordrecht, NL, vol. 22, No. 2, Aug. 2002, pp. 139-151.

"ITU-T Recommendation G.992.5—Series G: Transmission Systems and Media, Digital Systems and Networks", International Telecommunication Union, ADSL2, May 2003, 92 pages.

"ITU-T Recommendation G.992.3," International Telecommunication Union, ADSL2, Jan. 2005, 436 pages.

"VDSL2 ITU-T Recommendation G.993.2," International Telecommunication Union, Feb. 2006, 252 pages.

"Sunset xDSL: Prequalification of ADSL Circuits with ATU-C Emulation," Sunrise Telecom Inc., Application Series, 2001, San Jose, USA, p. 3, available at http://www.sunrisetelecom.com/technotes/APP-xDSL-8B.pdf.

International Search Report for International (PCT) Patent Application No. PCT/US2005/036015, mailed Feb. 8, 2006.

Written Opinion for International (PCT) Patent Application No. PCT/US2005/036015, mailed Feb. 8, 2006.

International Preliminary Report on Patentability for International (PCT) Patent Application No. PCT/US2005/036015, mailed Apr. 26, 2007.

Examiner's First Report for Australian Patent Application No. 2005296086, mailed Jun. 24, 2009.

Examiner's First Report for Australian Patent Application No. 2011201250 mailed May 13, 2013.

Examiner's Report for Canadian Patent Application No. 2,580,280, mailed Sep. 14, 2012.

Notification of the First Office Action (including translation) for Chinese Patent Application No. 200580032703, mailed Sep. 25, 2009.

Official Action (including translation) for Chinese Patent Application No. 200580032703, dispatched May 18, 2011.

Official Action (including translation) for Chinese Patent Application No. 200580032703.1, dispatched Mar. 28, 2012.

Decision of Refusal (including translation) for Chinese Patent Application No. 200580032703.1, dispatched Sep. 5, 2012.

Official Action for European Application No. 05807443.6, mailed Mar. 6, 2013.

First Examination Report for Indian Patent Application No. 1208/KOLNP/2007, mailed Mar. 18, 2013.

Official Action (translation only) for Korean Patent Application No. 10-2007-7008270, mailed Jun. 30, 2011.

Notice of Allowance (including translation) for Korean Patent Application No. 10-2007-7008270, mailed Mar. 29, 2012.

Official Action (translation only) for Korean Patent Application No. 10-2010-7022463, mailed Jun. 30, 2011.

Notice of Allowance (including translation) for Korean Patent Application No. 10-2010-7022463, mailed Mar. 29, 2012.

Official Action (including translation) for Japanese Patent Application No. 2007-535818, dispatched Jul. 11, 2011.

Notice of Allowance for Japanese Patent Application No. 2007-535818, dispatched Dec. 12, 2011.

Official Action (including translation) for Japanese Patent Application No. 2008-264540, dispatched Jul. 11, 2011.

Official Action (including translation) for Japanese Patent Application No. 2008-264540, dispatched Dec. 12, 2011.

Notice of Allowance for Japanese Patent Application No. 2008-264540, mailed Mar. 26, 2012.

Invitation to Pay Additional Fees (including partial international search report) for International (PCT) Patent Application No. PCT/US2007/066522, mailed Feb. 6, 2008.

International Search Report for International (PCT) Patent Application No. PCT/US2007/066522, mailed Apr. 14, 2008.

Written Opinion for International (PCT) Patent Application No. PCT/US2007/066522, mailed Apr. 14, 2008.

International Preliminary Report on Patentability for International (PCT) Patent Application No. PCT/US2007/066522, mailed Oct. 23, 2008.

Examiner's First Report on Australian Patent Apllication No. 2007257055, mailed Mar. 30, 2010.

Official Action (including translation) for Chinese Patent Application No. 200780012891.0, dispatched Mar. 16, 2011.

(56) **References Cited**

OTHER PUBLICATIONS

Notification of the Second Office Action (including translation) for Chinese Patent Application No. 200780012891.0, dispatched Mar. 7, 2012.
Notification of the Second Office Action (including translation) for Chinese Patent Application No. 200780012891.0, dispatched Dec. 12, 2012.
Official Action for Columbian Patent Application No. 08-109-377, dated Nov. 5, 2010.
Examination Report for European Patent Application No. 07811844.5, mailed Apr. 1, 2009.
Official Action for European Patent Application No. 07811844.5, dated Jul. 9, 2010.
Official Action for European Patent Application No. 07811844.5, dated Dec. 21, 2010.
Official Action for European Patent Application No. 07811844.5, dated Dec. 18, 2012.
European Search Report and Opinion for European Patent Application No. 10000017.3, dated Mar. 17, 2010.
Official Action for European Patent Application No. 10000017.3, dated Nov. 3, 2010.
European Search Report and Opinion for European Patent Application No. 10000016.5, dated Mar. 3, 2010.
Official Action for European Patent Application No. 10000016.5, dated Nov. 3, 2010.
Official Action for European Patent Application No. 10000016.5, dated Dec. 22, 2011.
Communication Under Rule 71(3) EPC—Intention to Grant for European Patent Application No. 10000016.5, dated Dec. 18, 2012.
Decision to Grant a European Patent Pursuant to Article 97(1) EPC for European Patent Application No. 10000016.5, dated May 31, 2013.
Official Action for Japanese Patent Application No. 2009-505623, dispatched Apr. 4, 2011.
Official Action (including translation) for Japanese Patent Application No. 2009-505623, dispatched Oct. 31, 2011.
Official Action for Japanese Patent Application No. 2010-017356, dispatched Apr. 18, 2011.
Official Action (including translation) for Japanese Patent Application No. 2010-017356, dispatched Aug. 29, 2011.
Decision of Final Rejection for Japanese Patent Application No. 2010-017356, dispatched Apr. 23, 2012.
Official Action for Japanese Patent Application No. 2012-042978, dispatched Jun. 3, 2013.
Official Action (including translation) for Mexican Patent Application No. MX/a/2008/012505, dated Apr. 22, 2010.
Official Action (including translation) for Mexican Patent Application No. MX/a/2008/012505, dated Aug. 9, 2011.
Official Notification of Intent to Grant (including translation) for Mexican Patent Application No. MX/a/2008/012505, mailed Apr. 3, 2012.
Official Action for U.S. Appl. No. 11/246,163, mailed Feb. 24, 2009.
Official Action for U.S. Appl. No. 11/246,163, mailed Dec. 9, 2009.
Notice of Allowability for U.S. Appl. No. 11/246,163, mailed Sep. 7, 2010.
Notice of Allowability for U.S. Appl. No. 12/761,586, mailed Oct. 6, 2010.
Notice of Allowability for U.S. Appl. No. 12/853,020, mailed Oct. 6, 2010.
Official Action for U.S. Appl. No. 12/901,699, mailed Jan. 6, 2012.
Notice of Allowance for U.S. Appl. No. 12/901,699, mailed Jul. 27, 2012.
Official Action for U.S. Appl. No. 13/567,261, mailed Sep. 28, 2012.
Notice of Allowance for U.S. Appl. No. 13/567,261, mailed May 21, 2013.
Official Action for U.S. Appl. No. 12/295,828, mailed Jan. 5, 2012.
Notice of Allowance for U.S. Appl. No. 12/295,828, mailed Aug. 17, 2012.
Notice of Allowance for U.S. Appl. No. 12/783,758, mailed Dec. 26, 2012.
Official Action for U.S. Appl. No. 12/760,728, mailed Apr. 27, 2012.
Official Action for U.S. Appl. No. 12/760,728, mailed Jan. 2, 2013.
Official Action for U.S. Appl. No. 12/760,728, mailed Jun. 20, 2013.
Official Action for U.S. Appl. No. 12/783,765, mailed May 17, 2012.
Official Action for U.S. Appl. No. 12/783,765, mailed Dec. 17, 2012.
Notice of Allowance for U.S. Appl. No. 12/783,765, mailed May 9, 2013.
Official Action for U.S. Appl. No. 13/766,059, mailed Oct. 2, 2013.
Official Action for U.S. Appl. No. 12/760,728, mailed Oct. 2, 2013.
Notice of Allowance for U.S. Appl. No. 12/760,728, mailed Oct. 21, 2013.

* cited by examiner

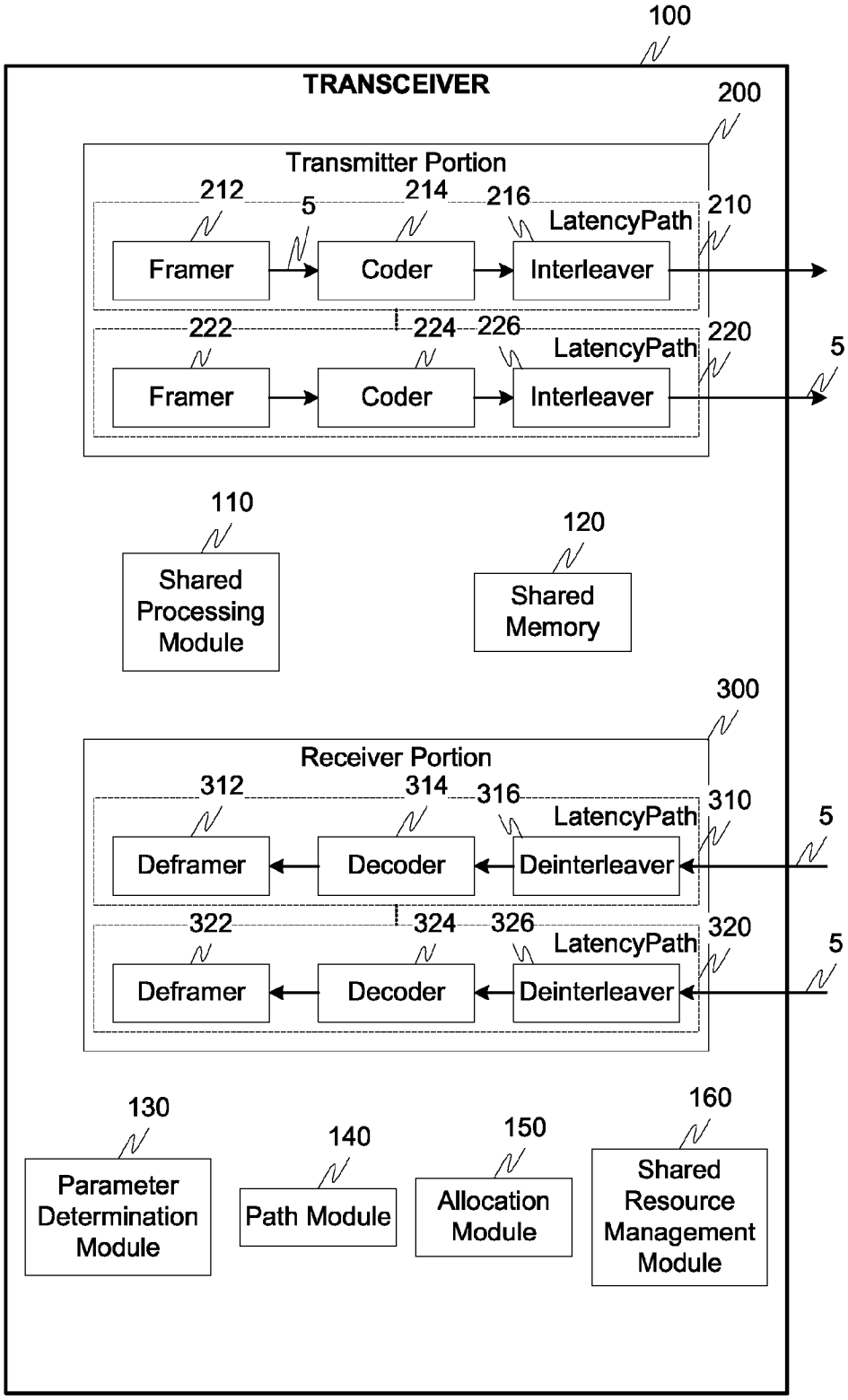

100
TRANSCEIVER
200
Transmitter Portion
212
5
214
216
LatencyPath
210
Framer
Coder
Interleaver
222
224
226
LatencyPath
220
5
Framer
Coder
Interleaver
110
Shared Processing Module
120
Shared Memory
300
Receiver Portion
312
314
316
LatencyPath
310
5
Deframer
Decoder
Deinterleaver
322
324
326
LatencyPath
320
5
Deframer
Decoder
Deinterleaver
130
Parameter Determination Module
140
Path Module
150
Allocation Module
160
Shared Resource Management Module

Fig. 1

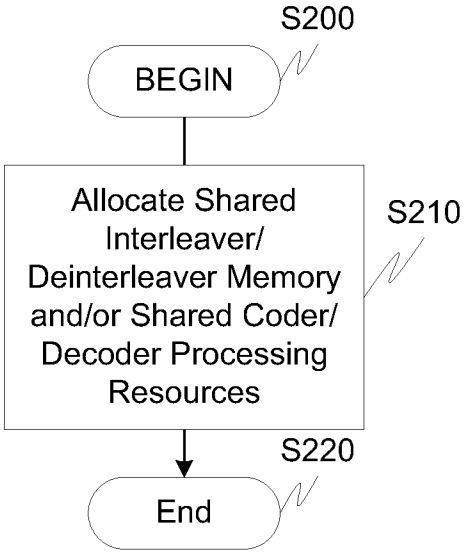

S200
BEGIN
Allocate Shared Interleaver/ Deinterleaver Memory and/or Shared Coder/ Decoder Processing Resources
S210
S220
End

Fig. 2

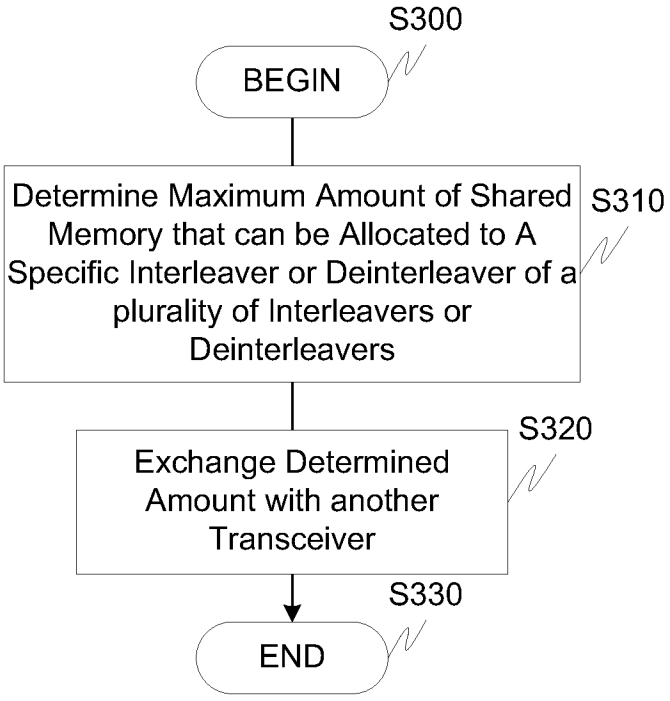

S300
BEGIN
Determine Maximum Amount of Shared Memory that can be Allocated to A Specific Interleaver or Deinterleaver of a plurality of Interleavers or Deinterleavers
S310
Exchange Determined Amount with another Transceiver
S320
S330
END

Fig. 3

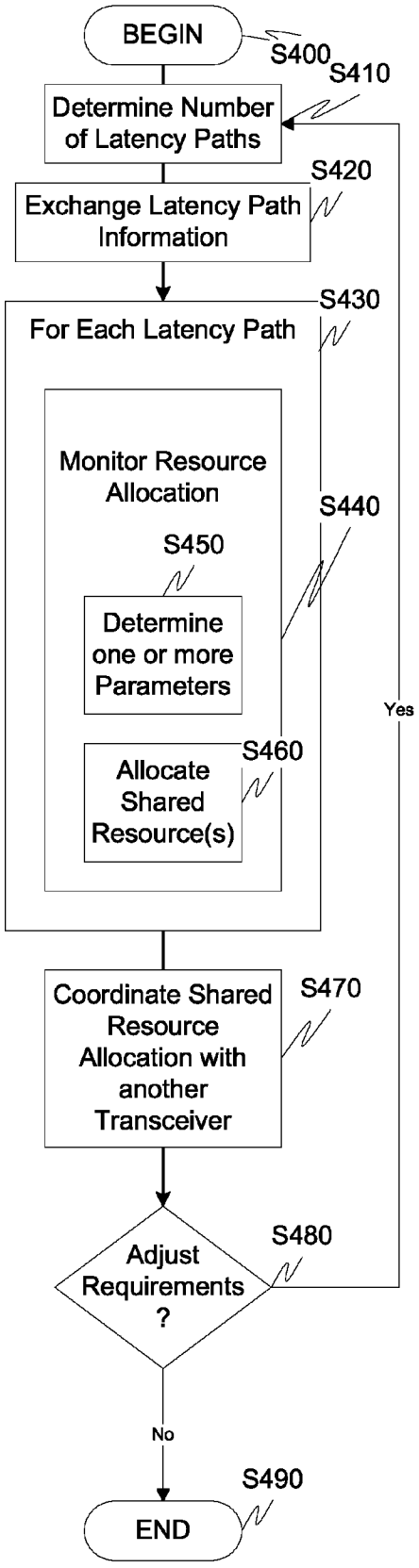

BEGIN
S400
S410
Determine Number of Latency Paths
S420
Exchange Latency Path Information
S430
For Each Latency Path
Monitor Resource Allocation
S440
S450
Determine one or more Parameters
S460
Allocate Shared Resource(s)
Yes
S470
Coordinate Shared Resource Allocation with another Transceiver
S480
Adjust Requirements ?
No
S490
END

Fig. 4

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

This application is a Continuation of U.S. application Ser. No. 13/567,261, filed Aug. 6, 2012, now U.S. Pat. No. 8,495,473, which is a Continuation of U.S. application Ser. No. 12/901,699, filed Oct. 11, 2010, now U.S. Pat. No. 8,276,048, which is a Continuation of Ser. No. 12/761,586, filed Apr. 16, 2010, now U.S. Pat. No. 7,844,882, which is a Continuation of U.S. application Ser. No. 11/246,163 filed Oct. 11, 2005, now U.S. Pat. No. 7,831,890, which claims the benefit of and priority under 35 U.S.C. §119(e) to U.S. Patent Application No. 60/618,269, filed Oct. 12, 2004, entitled "Sharing Memory and Processing Resources in DSL Systems," each of which are incorporated herein by reference in their entirety.

BACKGROUND

1. Field of the Invention

This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

2. Description of Related Art

U.S. Pat. Nos. 6,775,320 and 6,778,596 describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

As described in U.S. Pat. No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a combination thereof and a shared memory designed to be allocated to a plurality of the modules.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

FIG. **1** is a functional block diagram illustrating an exemplary transceiver according to this invention;

FIG. **2** is a flowchart outlining an exemplary method of sharing resources according to this invention;

FIG. **3** is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

FIG. **4** is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used interchangeably.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100** that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver **100** can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100**. The transceiver **100** includes a transmitter portion **200** and a receiver portion **300**. The transmitter portion **200** includes one or more latency paths **210**, **220**, ... Similarly, the receiver portion **300** includes one or more latency paths **310**, **320**, ... Each of the latency paths in the transmitter portion **200** includes a framer, coder, and interleaver designated as **212**, **214**, **216** and **222**, **224** and **226**, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as **312**, **314**, **316** and **322**, **324**, and **326**, respectively. The transceiver **100** further includes a shared processing module **110**, a shared memory **120**, a parameter determination module **130**, a path module **140**, an allocation module **150**, and a shared resource management module **160**, all interconnected by one or more links (not shown).

In this exemplary embodiment, the transceiver **100** is illustrated with four total transmitter portion and receiver portion latency paths, i.e., **210**, **220**, **310**, and **320**. The shared memory **120** is shared amongst the two transmitter portion interleavers **216** and **226** and two receiver portion deinterleavers **316** and **326**. The shared processing module **110**, such

as a shared coding module, is shared between the two transmitter portion coders **214** and **224** and the two receiver portion decoders **314** and **324**.

While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path **210**, the interleaver **216** could be allocated a portion of the shared memory **120**, while the coder **214** could be allocated to a dedicated processing module, vice versa, or the like.

In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory **120**, and a coding module, such as shared processing module **110**. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module **110**, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory **120** to an interleaver, such as interleaver **216** in the transmitter portion of the transceiver and allocate a second portion of the shared memory **120** to a deinterleaver, such as **316**, in the receiver portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory **120**, and be designed to allocate a first portion of shared memory **120** to a first interleaver, e.g., **216**, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., **226**, in the transmitter portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory **120** to a first deinterleaver, e.g., **316**, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., **326**, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory **120**.

Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module **140**, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module **130** then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module **150** allocates a portion of the shared memory **120** to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management **160**, the transceiver **100** transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require N*D=255*64=16 Kbytes of interleaver memory at the transmitter (or deinterleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

A second transmitter portion or receiver portion latency path may carry an internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). This latency path will require N*D=128*32=4 Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least (16+4)=20 Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with N=255/R=16 and N=128/R=8.

According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). Each latency path will require N*D=128*32=4 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with N=128/R=16, N=128/R=8 and N=128/R=8.

Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only 2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes (N=200) with 10 checkbytes (R=10) and interleaving/deinterleaving using an interleaver depth of 50 (D=50). Each latency path will require N*D=200*50=10 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

- Number of supported transmitter and receiver latency paths=3
- Max Interleaver Memory for latency path #1=16 Kbytes
- Max Interleaver Memory for latency path #2=16 Kbytes
- Max Interleaver Memory for latency path #3=16 Kbytes
- Maximum total/shared memory for all latency paths=20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1—Video: N=255, R=16, D=64
latency path #2—Video: N=128, R=8, D=32
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would result in a total interleaver memory of 20 kbytes.

Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1—Video: N=200, R=10, D=50
latency path #2—Video: N=200, R=10, D=50
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would also result in a total interleaver memory of 20 kbytes.

Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

FIG. **2** outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step **S200** and continues to step **S210**. In step **S210**, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step **S220** where the control sequence ends.

FIG. **3** outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step **S310**. In step **S310**, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is deter-

mined. Next, in step S**320**, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S**330** where the control sequence ends.

FIG. **4** outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S**400** and continues to step S**410**. In step S**410**, the number of latency paths are determined. Then, in step S**420**, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S**430**.

In step S**430**, and for each latency path, the steps in step **440** are performed.

In step S**440**, and while monitoring of allocation of resources is being performed, steps **450** and **460** are performed. More specifically, in step S**450**, one or more parameters associated with the communication system are determined. Then, in step S**460**, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S**470**.

In step S**470**, the allocation of shared resources is communicated to another transceiver. Next, in step S**480**, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S**410**. Otherwise, control jumps to step S**490** where the control sequence ends.

The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

The invention claimed is:

1. An apparatus comprising:

a multicarrier communications transceiver that is configured to perform a first interleaving function associated with a first latency path and perform a second interleaving function associated with a second latency path, the multicarrier communications transceiver being associated with a memory,

wherein the memory is allocated between the first interleaving function and the second interleaving function in accordance with a message received during an initialization of the transceiver and wherein at least a portion of the memory may be allocated to the first interleaving function or the second interleaving function at any one particular time depending on the message.

2. The apparatus of claim **1**, wherein the message is based on one or more communication parameters.

3. The apparatus of claim **2**, wherein at least one of the communication parameters is a data rate, a latency, an INP value, or a Bit Error Rate (BER).

4. The apparatus of claim **1**, wherein the transceiver is configured to transport one or more of video, internet access and voice data using a wired or wireless channel.

5. The apparatus of claim **1**, wherein the apparatus is a customer premises modem that is capable of transporting video.

6. The apparatus of claim 1, wherein the transceiver includes a shared processing module configured to provide processing resources to one or more of a plurality of coding and decoding modules.

7. The apparatus of claim 1, wherein the transceiver includes at least one digital signal processor.

8. The apparatus of claim 1, wherein the transceiver includes at least one ASIC.

9. The apparatus of claim 1, wherein a sum of a maximum amount of the memory that can be allocated to the first interleaving function and a maximum amount of the memory that can be allocated to the second interleaving function is more than a total amount of the memory.

10. An apparatus comprising:

a multicarrier communications transceiver that is configured to generate a message during an initialization of the transceiver, perform a first deinterleaving function associated with a first latency path, and perform a second deinterleaving function associated with a second latency path, the transceiver being associated with a memory,

wherein at least a portion of the memory may be allocated to the first deinterleaving function or the second deinterleaving function at any one particular time and wherein the generated message indicates how the memory has been allocated between the first deinterleaving function and second deinterleaving function.

11. The apparatus of claim 10, wherein the message is based on one or more communication parameters.

12. The apparatus of claim 11, wherein at least one of the communication parameters is a data rate, a latency, an INP value, or a Bit Error Rate (BER).

13. The apparatus of claim 10, wherein the transceiver is configured to transport one or more of video, internet access and voice data using a wired or wireless channel.

14. The apparatus of claim 10, wherein the apparatus is a linecard that is capable of transporting video.

15. The apparatus of claim 10, wherein the transceiver includes a shared processing module configured to provide processing resources to one or more of a plurality of coding and decoding modules.

16. The apparatus of claim 10, wherein the transceiver includes at least one digital signal processor.

17. The apparatus of claim 10, wherein the transceiver includes at least one ASIC.

18. The apparatus of claim 10, wherein a sum of a maximum amount of the memory that can be allocated to the first deinterleaving function and a maximum amount of the memory that can be allocated to the second deinterleaving function is more than a total amount of the memory.

19. A method of operating components of a telecommunications network, the components including: a first multicarrier communications transceiver located in a linecard and a second multicarrier communications transceiver located at a customer premises, the first transceiver being configured to perform a first deinterleaving function associated with a first latency path and perform a second deinterleaving function associated with a second latency path, the second transceiver being configured to perform a first interleaving function associated with the first latency path and perform a second interleaving function associated with the second latency path and each of the first and second transceivers being associated with a respective memory, the method comprising:

causing the first transceiver to allocate the memory associated with the first transceiver between the first deinterleaving function performed by the first transceiver and the second deinterleaving function performed by the first transceiver, wherein at least a portion of the memory associated with the first transceiver may be allocated to the first deinterleaving function performed by the first transceiver or the second deinterleaving function performed by the first transceiver at any one particular time; and

causing the first transceiver to transmit a message to the second transceiver during an initialization of the second transceiver, wherein the message indicates how the memory associated with the second transceiver is to be allocated between the first interleaving function performed by the second transceiver and the second interleaving function performed by the second transceiver and wherein at least a portion of the memory associated with the second transceiver may be allocated to the first interleaving function performed by the second transceiver or the second interleaving function performed by the second transceiver at any one particular time depending on the message.

20. The method of claim 19, wherein the message is transmitted or received using a wired or wireless channel and wherein the method further comprises causing the first transceiver to transport video, internet access and voice data using the wired or wireless channel.

21. The method of claim 19, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules within the first transceiver.

22. The method of claim 19, wherein the message is based on one or more communication parameters.

23. The method of claim 22, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate (BER).

24. The method of claim 19, wherein the telecommunications network is a DSL network.

25. The method of claim 19, wherein the first transceiver is included within a line card.

26. The method of claim 19, wherein the second transceiver is included within a customer premises modem.

27. The method of claim 19, wherein a sum of a maximum amount of the memory associated with the first transceiver that can be allocated to the first deinterleaving function performed by the first transceiver and a maximum amount of the memory associated with the first transceiver that can be allocated to the second deinterleaving function performed by the first transceiver is more than a total amount of the memory associated with the first transceiver.

28. The method of claim 19, wherein a sum of a maximum amount of the memory associated with the second transceiver that can be allocated to the first interleaving function performed by the second transceiver and a maximum amount of the memory associated with the second transceiver that can be allocated to the second interleaving function performed by the second transceiver is more than a total amount of the memory associated with the second transceiver.

* * * * *

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Frank Hargrave

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Frank Hargrave

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traffic path A channel, circuit, frequency band, line, switch, time slot, or trunk over which individual communications pass.

traffic shaping Allows the station sending information into an asynchronous transfer mode (ATM) network to:

- Specify the priority and throughput of information going into the network, and
- Monitor performance to meet required service levels.

traffic unit A synonym for *erlang* (*E*).

traffic usage recorder A device (or system) used to sample and record the occupancy of equipment, i.e., the amount of telephone traffic carried by a group, or several groups, of switches or trunks.

.trailer Information occupying the last several bytes of a block or packet. *Trailers* often contain checksums or other error control information.

train (1) A sequence of events or items, such as a *pulse train.* (2) To modify the behavior of a device based on external conditions, as in the *training* of an echo canceler for each new connected path.

transaction (1) An interaction between a client and a server. A sequence of messages between a master and client station required to perform a specific function. (2) The smallest complete action when using the Structured Query Language (SQL) to search or modify a database. (If any step in the transaction cannot be completed, the entire transaction fails, and all the intermediate steps in the transaction are undone.) (3) An entry in a database.

transaction code An identifier or symbol associated with a specific transaction and representing the action to be carried out.

For example, the letter *A* may be used as a transaction code for the operation "add," *D* may be "delete," and so on.

transceiver (1) A contraction of TRANSmitter and reCEIVER. A device that can both transmit and receive signals, such as cellular telephones, modems, and network interface controllers (NICs). Often NICs provide some form of collision detection as well. Also known as a *medium attachment unit* (*MAU*) in IEEE specifications. (2) In military communications, the combination of transmitting and receiving equipment which:

- Is housed in a common chassis or enclosure,
- Is usually designed for portable or mobile use,
- Uses common circuit components for both transmitting and receiving, and
- Provides half-duplex operation.

transceiver cable In Ethernet, a cable that attaches a terminal device to an Ethernet backbone cable (either 10Base2 or 10Base5).

transcoder A device that directly converts one digital code into another digital code, i.e., without returning the original code to an analog form before generating the new code.

For example, the conversion of μ255-law encoded pulse code modulation (PCM) to A-law PCM for transmission from the United States to countries in Europe.

transducer A device for converting energy from one form (heat, light, sound, temperature, electrical, etc.) to another for either measurement of a physical quantity or information transfer.

Examples of transducers include devices that:

- Convert sound pressure levels into electrical signals (microphones).
- Convert electrical signals into sound pressure waves (speakers).

transfer (1) The *movement of data* from one location to another. (2) The *passing of control* from one device to another. (3) In telephony, a switching system feature that allows a user to reassign a call to different end station.

transfer characteristics Those intrinsic parameters of an entity (system, subsystem, or device) which, when applied to the input of the entity, will fully describe its output. See also *transfer function.*

transfer delay A performance characteristic that expresses the amount of elapsed time required to send a message through a system. It includes not only the link's propagation time but any signal processing time required at either end of the link.

transfer function (1) A mathematical statement that describes the *transfer characteristics* of a system, subsystem, or device. (2) A rule (the *transfer characteristic*) describing how the output signal of circuit, device or system responds to an input signal. The rule may be stated in mathematical, graphical, or tabular terms. A *transfer function* is essentially the complex ratio of the output signal of the entity to the input signal.

When the *transfer function* (T) operates on the input (e_i), the output (e_o) is obtained. Given any two of these three entities (T, e_i, and e_o), the third can be obtained, that is,

$$T = e_o / e_i \,, \quad e_o = T \cdot e_i \,, \quad \text{or} \quad e_i = e_o / T$$

Simple transfer functions express the ratio of output to input signals when the imaginary part of the signals can be ignored, examples are voltage and current gains, reflection coefficients, transmission coefficients, and efficiency ratios. *Complex transfer functions* include the imaginary part and are frequency dependent, examples include filter response and envelope delay distortion. *Transfer functions* are frequently expressed in terms of amplitude vs. frequency and phase vs. frequency. (3) In an optical fiber, the complex mathematical function that expresses the ratio of the variation of the instantaneous power of the optical signal at the output of the fiber (P_o) to the instantaneous power of the optical signal that is launched into the fiber (P_i), as a function of modulation frequency.

transfer mode In telecommunications, the manner in which data are transmitted and/or switched in a network, i.e., synchronous vs. asynchronous, circuit switched vs. packet switched, and so on.

transfer rate The rate at which information is conveyed across a communications channel or circuit. *Transfer rate* is expressed in units per second (e.g., bits per second, characters per second, bytes per second, and so on). It may represent either the maximum number of units per second possible or the average number of units per second (including headers, trailers, and gaps between blocks). See also *baud.*

transfer rate of information bits (TRIB) The *average* transfer rate of actual, error-free, useful information (not including overhead, error bits, or retransmitted bits) through a device or series of devices. Mathematically, *TRIB* can be expressed as:

$$\text{TRIB} = \frac{\text{Number of information bits properly received}}{\text{Total time required to get the bits}}$$

Data compression increases the transfer rate by reducing the number of bits to be transmitted so that more information can be transferred in the same time. *TRIB* is also called the *throughput* or *data transfer rate.*

transfer ratio A dimensionless transfer function.

transfer time (1) The time it takes to switch from one process or device to an alternate. (2) In gas tube surge protectors, the amount of time required for the voltage across the gap to drop into the arc region after the initial gap conduction begins. (3) The amount of time required to transmit and receive a complete message.

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of an applied impulse. *See also:* electromagnetic compatibility. (T&D/PE) 430-1986w, 539-1990

(4) **(spectrum analyzer) (non-real time spectrum analyzer)** The peak value of the time response envelope divided by the spectrum amplitude (assumed flat within the bandpass) of an applied pulse. (IM) 748-1979w

impulse circuitry (nonlinear, active, and nonreciprocal waveguide components) A term given to the circuitry associated with either a step recovery or a dual mode varactor frequency multiplier. As charge is stored in the multiplier diode during each positive cycle of the input frequency and released during each negative cycle, a magnetic field is built up in an impulse inductor that stores all the circuit energy as charge approaches zero. Multiplication occurs when the inductor releases its energy in the form of an impulse voltage across the diode at the time of switching or high-impedance recovery. (MTT) 457-1982w

impulse current (current testing) Ideally, an aperiodic transient current that rises rapidly to a maximum value and falls usually less rapidly to zero. A rectangular impulse current rises rapidly to a maximum value, remains substantially constant for a specified time and then falls rapidly to zero. (PE/PSIM) 4-1978s

impulse currents (high voltage testing) Two types of impulse currents are dealt with. The first type has a shape which increases from zero to a crest value in a short time, and thereafter decreases to zero, either approximately exponentially or in the manner of a heavily damped sine curve. This type is defined by the virtual front time T1 and the virtual time to half-value T2. The second type has an approximately rectangular shape and is defined by the virtual duration of the peak and the virtual total duration. (PE/PSIM) 4-1978s

impulse current tests *See:* virtual time to half-value; impulse currents; value of the test current; virtual origin; virtual total duration of a rectangular impulse current; virtual duration.

impulse (shock) excitation A method of producing oscillator current in a circuit in which the duration of the impressed voltage is relatively short compared with the duration of the current produced. *See also:* oscillatory circuit. (AP/BT/ANT) 145-1983s, 182-1961w

impulse flashover voltage (1) (insulators) The crest value of the impulse wave that, under specified conditions, causes flashover through the surrounding medium. (EEC/IEPL) [89]

(2) **(surge arresters)** The crest voltage of an impulse causing a complete disruptive discharge through the air between electrodes of a test specimen. *See also:* insulator; critical impulse flashover voltage. (PE) [8], 64

impulse flashover volt-time characteristic A curve plotted between flashover voltage for an impulse and time to impulse flashover, or time lag of impulse flashover. *See also:* insulator. (PE/T&D) [10]

impulse-forced response (automatic control) The total (transient plus steady-state) time response resulting from an impulse at the input. *Synonym:* impulse response. (PE/EDPG) [3]

impulse generator A standard reference source of broadband impulse energy. (EMC) 263-1965w

impulse inertia (surge arresters) The property of insulation whereby more voltage must be applied to produce disruptive discharge, the shorter the time of voltage application. (PE) [8], 64

impulse insulation level An insulation strength expressed in terms of the crest value of an impulse withstand voltage. *See also:* basic impulse insulation level. (EEC/LB) [100]

impulse noise (1) (A) (data transmission) (overhead-power-line corona and radio noise) Noise characterized by transient disturbances separated in time by quiescent intervals. *Notes:* 1. The frequency spectrum of these disturbances are substantially uniform over the useful pass band of the transmission system. 2. The same source may produce impulse noise in one system and random noise in a different system. *See also:* signal-to-noise ratio. **(B)** Any burst of noise that produces a voltage exceeding the root-mean-square (rms) noise voltage (i.e., the mean noise as measured with a standard noise measuring set using C-message weighting) by a given magnitude. Impulse noise is a spike that exceeds the rms value of the background or quantizing noise by at least 12 dB. The impulse noise counter registers the number of instances in which the measured noise exceeds a preset threshold. (T&D/PE/AP/COM/TA/ANT) 539-1990, 599-1985, 145-1983, 973-1990

(2) A component of the received noise signal that is much greater in amplitude than the normal peaks of the message circuit noise, and that occurs as short-duration spikes or energy bursts. (PE/IC) 1143-1994r

(3) Noise characterized by electrical pulses of high amplitude and narrow width, often originating from switching devices or electrical storms. (C) 610.7-1995

(4) Any burst of noise that produces a voltage exceeding the rms value of the background or quantizing noise by more than 12 dB. (COM/TA) 743-1995

(5) Noise characterized by transient disturbances. Impulses exceeding a specified threshold are counted for a specific duration with an impulse noise counter designed in accordance with IEEE Std 743-1984. (COM/TA) 1007-1991r

impulse-noise selectivity (receiver) A measure of the ability to discriminate against impulse noise. (VT) [37]

impulse protective level For a defined wave shape, the higher of the maximum sparkover value or the corresponding discharge-voltage value. (SPD/PE) C62.11-1999

impulse protective volt-time characteristic The discharge-voltage-time response of the device to impulses of a designated wave shape and polarity, but of varying magnitudes. (SPD/PE) C62.11-1999

impulse radar A radar whose transmitted pulse consists of one or a few cycles of carrier, usually generated by application of a short video pulse to a wideband radio frequency (RF) amplifier (e.g., a traveling-wave tube) or directly to a wideband antenna (e.g., a dipole). (AES) 686-1997

impulse ratio (surge arresters) The ratio of the flashover, sparkover, or breakdown voltage of an impulse to the crest value of the power-frequency, sparkover, or breakdown voltage. (T&D/PE) [10], [8]

impulse relay (A) A relay that follows and repeats current pulses, as from a telephone dial. **(B)** A relay that operates on stored energy of a short pulse after the pulse ends. **(C)** A relay that discriminates between length and strength of pulses, operating on long or strong pulses and not operating on short or weak ones. **(D)** A relay that alternately assumes one of two positions as pulsed. **(E)** Erroneously used to describe an integrating relay. *See also:* relay. (PE/EM) 43-1974

impulse response (1) (linear network) The response, as a function of time, of a network when the excitation is a unit impulse. Hence, the impulse response of a network is the inverse Laplace transform of the network function in the frequency domain. (CAS) [13]

(2) **(fiber optics)** The function h(t) describing the response of an initially relaxed system to an impulse (Dirac-delta) function applied at time $t = 0$. The root-mean-square (rms) duration, σ_{rms}, of the impulse response is often used to characterize a component or system through a single parameter rather than a function:

$$\sigma_{rms} = [1/M_0 \int_{-\infty}^{\infty} (T-t)^2 h(t)dt]^{1/2}$$

where

$$M_0 = \int_{-\infty}^{\infty} h^{(t)dt}$$

$$T = 1/M_0 \int_{-\infty}^{\infty} th^{(t)dt}$$

Note: The impulse response may be obtained by deconvolving the input waveform from the output waveform, or as the

memory array (1) A matrix of memory locations arranged in a rectangular geometric pattern on an integrated circuit. (C) 610.10-1994w

(2) *See also:* array. (ED) 1005-1998

memory bank *See:* bank.

memory board A circuit board that provides random-access memory to a system. (C) 610.10-1994w

memory boundary The last address of an aligned data block. The maximum data block size that can be transferred by an IUT Master is the product of data width and data length. (C/BA) 896.4-1993w

memory buffer register A register in which a word is stored as it is read from memory or as it is written to memory. *Synonym:* memory data register. (C) 610.10-1994w

memory bus A bus connecting memory to the devices which can access it, including the processor and peripheral devices. (C) 610.10-1994w

memory capacity (1) The maximum number of bits that a memory is capable of storing. (ED) 641-1987w

(2) (software) The maximum number of items that can be held in a given computer memory; usually measured in words or bytes. (C) 610.12-1990

(3) *See also:* capacity. (ED) 1005-1998

(4) (electronic computation) *See also:* channel capacity; storage capacity.

memory cell (1) The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved. (ED) 641-1987w

(2) The combination of one or more single or merged transistors formed to provide a means of accessing, changing, and storing data. (ED) 1005-1998

memory compaction (A) A storage allocation technique in which the contents of all allocated storage areas are moved to the beginning of the storage space and the remaining storage blocks are combined into a single block. *Synonym:* garbage collection. **(B)** A storage allocation technique in which contiguous blocks of nonallocated storage are combined to form single blocks. (C) 610.12-1990

memory core *See:* magnetic core.

memory cycle (1) (test, measurement, and diagnostic equipment) The time required to read information from memory and replace it. (MIL) [2]

(2) A single complete access (read or write) of memory. (C) 610.10-1994w

memory data register *See:* memory buffer register.

memory device A device that contains only memory and implements configuration registers. (C/MM) 1155-1992

memory dump A display of the contents of all or part of a computer's internal storage, usually in binary, octal, or hexadecimal form. *See also:* static dump; selective dump; snapshot dump; dynamic dump; change dump. (C) 610.12-1990

memory image A series of bits that can be stored within a contiguous portion of transponder memory and that may be passed as a parameter within commands initiated by the roadside equipment (RSE). (SCC32) 1455-1999

memory integrated circuit An integrated circuit consisting of memory cells and usually including associated circuits such as signal amplification and address selection. (ED) 1005-1998

memory location A subdivision of a memory, including one or several memory cells, that is the smallest part of the memory that can be addressed. *Note:* The content of a memory location is usually called a bit, a byte, or a word, as appropriate. (ED) 1005-1998

memory management unit (MMU) A device that performs address translation between a CPU's virtual addresses and the physical addresses of some bus; typically, the bus represented by the root node. (C/BA) 1275-1994

memory map (1) A diagram that shows where programs and data are stored in a computer's memory. (C) 610.12-1990

(2) A list of all the current addresses in a computer. *Note:* This may indicate what is currently allocated, who is using it and where it is located. *Synonym:* memory map list. (C) 610.10-1994w

memory map list *See:* memory map.

memory mapping (A) The manner in which an address is translated into a physical address of a storage location. *See also:* biasing; segmenting; paging. **(B)** The process of translating addresses as in definition (A). (C) 610.10-1994

memory-mode agent An agent that communicates with others by using memory and/or I/O space on the parallel system bus. (C/MM) 1296-1987s

memory-mode system A system in which the agents communicate with one another with data structures in memory and/or I/O space. (C/MM) 1296-1987s

memory object (1) Either a file or shared memory object. When used in conjunction with *mmap*(), a memory object will appear in the address space of the calling process. (C/PA) 9945-1-1996

(2) Either a file or shared memory object. When used in conjunction with `Map_Memory`, `Open_And_Map_Shared_Memory`, or `Open_Or_Create_And_Map_Shared_Memory`, a memory object will appear in the address space of the calling process. (C) 1003.5-1999

memory organization The arrangement of memory cells, either by geometrical arrangement in rows and columns or by organization of the data to be stored. (ED) 1005-1998, 641-1987w

memory page A segment of transponder memory that is assigned a unique location by which it may be referenced. (SCC32) 1455-1999

memory relay (A) A relay having two or more coils, each of which may operate independent sets of contacts, and another set of contacts that remain in a position determined by the coil last energized. **(B)** Sometimes erroneously used for polarized relay. *See also:* relay. (EEC/REE) [87]

memory-resident Managed by the implementation in such a way as to provide an upper bound on memory access times. (C/PA) 9945-1-1996, 1003.5-1999

memory space The address space used for accessing physical memory devices for storage and retrieval of code and data. (C/MM) 1296-1987s

memory window The difference in threshold voltage between the low- and high-conductance logic states of a memory cell. (ED) 641-1987w

MENTOR A block-structured language used widely in computer-aided instruction; characterized by its ability to model a student's knowledge. (C) 610.13-1993w

menu (1) A list of options available for selection by the user of a computer system. *Synonyms:* display menu; help menu; menu selection. (C) 610.2-1987, 610.6-1991w

(2) A rectangular visual user interface control containing a group of controls used to select an action from a group of choices. (C) 1295-1993w

menu bar A visual user interface control that is the bounded area near the top of a window, below the title bar, and above the rest of the window that contains cascade buttons that provide access to other menus. (C) 1295-1993w

menu by-pass In a menu-driven system, a feature that permits advanced users to perform functions in a command-driven mode without selecting options from the menus. (C) 610.12-1990

menu-driven Pertaining to a system or mode of operation in which the user directs the system through menu selections. *Contrast:* command-driven. *See also:* menu by-pass. (C) 610.12-1990

menu selection (A) The process of choosing an item from a menu. **(B)** The item chosen from a menu. (C) 610.2-1987

mercury-arc converter, pool-cathode *See:* pool-cathode mercury-arc converter; oscillatory circuit.

mercury-arc rectifier A gas-filled rectifier tube in which the gas is mercury vapor. *See also:* rectification. (ED) [45], [84]

node equations (networks) Any set of equations (of minimum number) such that the independent node voltages of a specified network may be determined from the impressed currents. *Notes:* 1. The number of node equations for a given network is not necessarily the same as the number of mesh or loop equations for that network. 2. Notes for mesh or loop equations, with appropriate changes, apply here. *See also:* network analysis. (Std100) 270-1966w

node_id (1) A 16 b value that determines the initial node address space. On some buses, the node_id value has two components: a *bus_id* field specifies one of 1024 bus address and an *offset_id* field specifies one of 64 node positions on the bus. During system initialization, software is expected to assign unique node_id values to nodes within a system. (C/MM) 1212-1991s

(2) A 16 b number that defines the initial node address space. During system initialization, systemwide unique node_id values may be assigned to nodes within a tightly coupled system. (C/BA) 896.9-1994w, 896.3-1993w

(3) A 16 b number that determines the node address space. After system initialization, unique node_id values have been assigned to all nodes within a tightly coupled system. The node_id is the part of the 64 b address that is used for routing packets. (C/MM) 1596-1992

(4) A unique 16 b number that distinguishes the node from other nodes in the system. The ten most significant bits of node_id are the same for all nodes on the same bus; this is the bus_id. The six least-significant bits of node_id are unique for each node on the same bus; this is called the physical_id. (C/MM) 1394-1995

(5) A 16-bit number that uniquely differentiates a node from all other nodes within a group of interconnected buses. The ten most significant bits of node ID are the same for all nodes on the same bus, i.e., the bus ID. The six least significant bits of node ID are unique for each node on the same bus; this is called the physical ID. The physical ID is assigned as a consequence of bus initialization. (C/MM) 1394a-2000

node index A text listing, often indented, of the nodes in an IDEF0 model, shown in outline order. Same meaning and node content as a node tree. (C/SE) 1320.1-1998

node interface A link interface on a switch. *See also:* link interface; switch. (C/BA) 1355-1995

node letter The letter that is the first character of a node number. (C/SE) 1320.1-1998

node name A text string of the form "`driver-name@unit-address:device-arguments`", which identifies a device node within the address space of its parent. (C/BA) 1275-1994

node number An expression that unambiguously identifies a function's position in a model hierarchy. A node number is constructed by concatenating a node letter, the diagram number of the diagram that contains the box that represents the function, and the box number of that box. (C/SE) 1320.1-1998

node ROM A range of register addresses that are mapped to address offsets 1024 to 2047. (C/BA) 896.10-1997, 896.2-1991w

node signal (network analysis) A variable X_k associated with node k. (CAS) 155-1960w

node tree A graphical listing of the nodes of an IDEF0 model, showing parent-child relationships as a graphical tree. Same meaning and node content as a node index. (C/SE) 1320.1-1998

node voltage (networks) The voltage from a reference point to any junction point (node) in a network. *Note:* The assumptions of lumped-network theory are such that the path of integration is immaterial. (Std100) 270-1966w

no-fill mode In text formatting, an operating mode in which no justification is performed. (C) 610.2-1987

no-go *See:* go/no-go.

noise (1) **(analog computer)** Unwanted disturbances superimposed upon a useful signal, which tend to obscure its information content. Random noise is the part of the noise that is unpredictable, except in a statistical sense. (C) 165-1977w

(2) **(A) (general) (data transmission)** An undesired disturbance within the useful frequency band. *Note:* Undesired disturbances within the useful frequency band produced by other services may be called interference. **(B)** Any unwanted disturbance in a system, such as random variations in voltage or current, or extra bits in data. **(C)** Any unwanted variation in a signal. *See also:* intermodulation noise; crosstalk; Gaussian noise; white noise; impulse noise. (PE) 599-1985

(3) **(phototubes)** The random output that limits the minimum observable signal from the phototube. *See also:* phototube. (NPS) 175-1960w, 398-1972r

(4) **(facsimile)** Any extraneous electric disturbance tending to interfere with the normal reception of a transmitted signal. (COM) 168-1956w

(5) **(hybrid computer linkage components)** Unwanted disturbances superimposed upon a useful signal that tends to obscure its information content expressed in millivolts peak and referred to the input voltage. (C) 166-1977w

(6) **(electrical noise)** Unwanted electrical signals that produce undesirable effects in the circuits of the control systems in which they occur. (IA/PE/T&D/ICTL/EDPG) 518-1982r, 1050-1996, 1250-1995

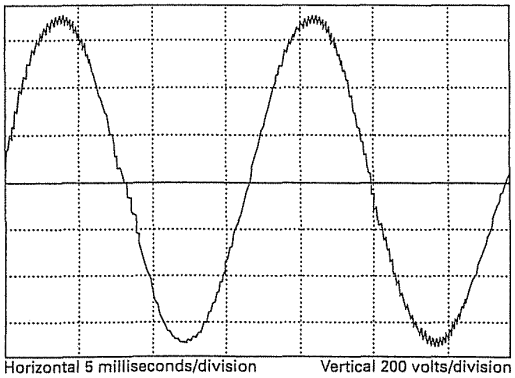
(7) **(oscilloscopes)** Any extraneous electric disturbance tending to interfere with the normal display. (IM) 311-1970w

(8) **(broadband local area networks)** Any unwanted-signal in a communications system. White noise (or random noise) is random energy (e.g.,shot noise and thermal noise) that has a uniform distribution of energy across the band-pass. The analogy for white noise is white light. Johnson noise (thermal) is the noise generated by electron movement (current through a resistor) above absolute zero. The noise level is proportional to temperature. Shot noise is the type of unrandom noise generated when current flows across an abrupt junction. Shot noise is characteristic of semiconductor devices. (LM/C) 802.7-1989r

(9) **(image processing and pattern recognition)** Irrelevant data that hamper recognition and interpretation of data of interest. (C) 610.4-1990w

(10) Any deviation between the output signal (converted to input units) and the input signal, except deviations caused by linear time invariant system response (gain and phase shift), a dc level shift, or an error in the sample rate. For example, noise includes the effects of random errors, fixed pattern errors, nonlinearities and time base errors (fixed error in sample time and aperture uncertainty). (IM/WM&A) 1057-1994w

(11) Electrical noise is unwanted electrical signals that produce undesirable effects in the circuits of the control systems in which they occur. See figure below.



noise example

(IA/PE/SPD/PSE) 1100-1992s, C62.48-1995

(12) Undesirable sound emissions or undesirable electromagnetic signals/emissions. (PE/SUB) 1127-1998

(13) Unwanted electrical signals in the circuits of the control systems in which they occur. (SCC22) 1346-1998

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How to Use This Dictionary

The terms defined in this dictionary are listed in alphabetical order. Terms made up of more than two words appear in the order most familiar to the people who use them. In some cases cross-references are given.

Some terms take on different meanings in different fields. When this happens the different definitions are numbered, identified as to area of origin, coded, and listed under the main entry.

If a reader wants to know the source of a definition he need only look up the code number following the definition in the SOURCES section that appears at the back of the book between pages 1112 and 1129.

of computer storage, a prefix indicating 2^{20}, or 1 048 576. 564

Meissner oscillator. An oscillator that includes an isolated tank circuit inductively coupled to the input and output circuits of an amplifying device to obtain the proper feedback and frequency. *See:* **oscillatory circuit.** 111

mel. A unit of pitch. By definition, a simple tone of frequency 1000 hertz, 40 decibels above a listener's threshold, produces a pitch of 1000 mels. *Note:* The pitch of any sound that is judged by the listener to be n times that of the 1-mel tone is n mels. 176

melting channel. The restricted portion of the charge in a submerged resistor or horizontal-ring induction furnace in which the induced currents are concentrated to effect high energy absorption and melting of the charge. *See:* **induction heating.** 14, 114

melting-speed ratio (of a fuse) (power switchgear). A ratio of the current magnitudes required to melt the current responsive element at two specified melting times. *Notes:* (1) Specification of the current wave shape is required for time less than one-tenth of a second. (2) The lower melting time in present use is 0.1 second, and the higher minimum melting current times are 100 seconds for low-voltage fuses and 300 or 600 seconds, whichever specified, for high-voltage fuses. 103

melting time (1)(of a fuse) (power switchgear). The time required for overcurrent to sever the current-responsive element. 103

(2)(protection and coordination of industrial and commercial power systems). The time required to melt the current-responsive element on a specified overcurrent. Where the fuse is current limiting in less than half-cycle, the melting time may be approximately half or less of the clearing time. *Syn:* **pre-arcing. See figure under arcing time.** 504

membrane potential. The potential difference, of whatever origin, between the two sides of a membrane. *See:* **electrobiology.** 192

memory (electronic computation). *See:* **storage; storage medium.**

memory action (of a relay). A method of retaining an effect of an input after the input ceases or is greatly reduced, so that this input can still be used in producing the typical response of the relay. *Note:* For example, memory action in a high-speed directional relay permits correct response for a brief period after the source of voltage input necessary to such a response is short-circuited. 103

memory capacity (electronic computation). *See:* **storage capacity.**

memory cycle (test, measurement and diagnostic equipment). The time required to read information from memory and replace it. 54

memory relay. (1) A relay having two or more coils, each of which may operate independent sets of contacts, and another set of contacts that remain in a position determined by the coil last energized. (2) Sometimes erroneously used for polarized relay. *See:* **relay.** 259

menu (computer applications). A list of options available for selection by the user of a computer system. *See:* **help menu; menu selection.** 571

menu selection (computer applications). (1) The process of choosing an item from a menu. (2) The item chosen from a menu. 571

mercury-arc converter, pool-cathode. *See:* **pool-cathode mercury-arc converter; oscillatory circuit.**

mercury-arc rectifier. A gas-filled rectifier tube in which the gas is mercury vapor. *See:* **rectification.** 244, 190

mercury cells. Electrolytic cells having mercury cathodes with which deposited metals form amalgams. 328

mercury-contact relays. (1) mercury plunger relay: A relay in which the magnetic attraction of a floating plunger by a field surrounding a sealed capsule displaces mercury in a pool to effect contacting between fixed electrodes. **(2) mercury-wetted-contact relay:** A form of reed relay in which the reeds and contacts are glass enclosed and are wetted by a film of mercury obtained by capillary action from a mercury pool in the base of a glass capsule vertically mounted. **(3) mercury-contact relay:** A relay mechanism in which mercury establishes contact between electrodes in a sealed capsule as a result of the capsule's being tilted by an electromagnetically actuated armature, either on pick-up or dropout or both. *See:* **mercury relay.** 341

mercury fluorescent lamp (illuminating engineering). An electric discharge lamp having a high-pressure mercury arc in an arc tube, and an outer envelope coated with a fluorescing substance (phosphor) which transforms some of the ultraviolet energy generated by the arc into light. 167

mercury-hydrogen spark-gap converter (dielectric heater usage). A spark-gap generator or power source which utilizes the oscillatory discharge of a capacitor through an inductor and a spark gap as a source of radio-frequency power. The spark gap comprises a solid electrode and a pool of mercury in a hydrogen atmosphere. *See:* **induction heating.** 14, 114

mercury lamp (illuminating engineering). A high intensity discharge (HID) lamp in which the major portion of the light is produced by radiation from mercury operating at a partial pressure in excess of $1.013 \times 10^5 Pa$(1 atmosphere). Includes clear, phosphor-coated (mercury-fluorescent), and self-ballasted lamps. 167

mercury-lamp ballast. *See:* **ballast.**

mercury-lamp transformer (series type). *See:* **constant-current (series) mercury-lamp transformer.**

mercury motor meter. A motor-type meter in which a portion of the rotor is immersed in mercury, which serves to direct the current through conducting portions of the rotor. *See:* **electricity meter.** 341

mercury oxide cell. A primary cell in which depolarization is accomplished by oxide of mercury. *See:* **electrochemistry.** 341

mercury-pool cathode (gas tube). A pool cathode consisting of mercury. 244, 190

bance or a change in reference input. *See:* **control system, feedback.** 219, 206, 54

stirring effect (induction heater usage). The circulation in a molten charge due to the combined forces of motor and pinch effects. *See:* **induction heating; motor effect; pinch effect.** 14, 114

stop (limit stop). A mechanical or electric device used to limit the excursion of electromechanical equipment. *See:* **limiter circuit.** 9

stop band (circuits and systems). A band of frequencies that pass through a filter with a substantial amount of loss (relative to other frequency bands such as a pass band). 67

stop-band ripple (circuits and systems). The difference between maxima and minima of loss in a filter stop band. 67

stop dowel (rotating machinery). A pin fitted into a hole to limit motion of a second part. 63

stop element (data transmission). In a character transmitted in a start-stop system, the last element in each character, to which is assigned a minimum duration, during which the receiving equipment is returned to its rest condition in preparation for the reception of the next character. The stop element is a marking signal. 59

stop-go pulsing (telephone switching systems). A method of pulsing control wherein the pulsing-operation may take place in stages, and the sending end is arranged to pulse the digits continuously unless or until the stop-pulsing signal is received. *Note:* When this occurs, the pulsing of the remaining digits is suspended until the sending end receives a start-pulsing signal. 55

stop joint (power cable joint). A joint which is designed to prevent any transfer of dielectric fluid between the cables being joined. 34

stop lamp (illuminating engineering). A lighting device giving a steady warning light to the rear of a vehicle or train of vehicles, to indicate the intention of the operator to diminish speed or to stop. 167

stop-motion switch (elevators). *See:* **machine final-terminal stopping device.**

stop or throttle valve(s) (control systems for steam turbine-generator units). Those valve(s) that normally provide fast interruption of the main energy input to the turbine. Throttle valves are sometimes used for turbine control during start-up. *Note:* The term stop valve is defined as an open or closed valve. A throttle valve has some portion of its opening through which it can modulate flow. 522

stopping device (5) (power system device function numbers). A control device used primarily to shut down an equipment and hold it out of operation. This device may be manually or electrically actuated, but excludes the function of electrical lockout on abnormal conditions. *See:* **lockout relay, device number 86.** 402

stopping off. The application of a resist to any part of a cathode or plating rack. *See:* **electroplating.** 328

stop-pulsing signal (telephone switching systems). A signal transmitted from the receiving end to the sending end of a trunk to indicate that the receiving end is not in a condition to receive pulsing. 55

stop-record signal (facsimile). A signal used for stopping the process of converting the electrical signal to an image on the record sheet. *See:* **facsimile signal (picture signal).** 12

stop signal (facsimile). A signal which initiates the transfer of a facsimile equipment condition from active to standby. *See:* **facsimile signal (picture signal).** 12

storable swimming or wading pool (National Electrical Code). A pool with a maximum dimension of 15 ft and a maximum wall height of 3 ft and is so constructed that it may be readily disassembled for storage and reassembled to its original integrity. 256

storage (electronic computation). (1) The act of storing information. (2) Any device in which information can be stored, sometimes called a memory device. (3) In a computer, a section used primarily for storing information. Such a section is sometimes called a memory or store (British). *Notes:* (A) The physical means of storing information may be electrostatic, ferroelectric, magnetic, acoustic, optical, chemical, electronic, electric, mechanical, etcetera, in nature. (B) Pertaining to a device in which data can be entered, in which it can be held, and from which it can be retrieved at a later time. *See:* **store.** 255, 77, 54

storage allocation (computing systems). The assignment of sequences of data or instructions to specified blocks of storage. 255, 77

storage assembly (storage tubes). An assembly of electrodes (including meshes) that contains the target together with electrodes used for control of the storage process, those that receive an output signal, and other members used for structural support. *See:* **storage tube.** 174

storage battery (National Electrical Code). A battery comprised of one or more rechargeable cells of the lead-acid, nickel-cadmium, or other rechargeable electrochemical types. 256

storage capacity. The amount of data that can be contained in a storage device. *Notes:* (1) The units of capacity are bits, characters, words, etcetera. For example, capacity might be "32 bits," "10 000 decimal digits," "16 384 words with 10 alphanumeric characters each." (2) When comparisons are made among devices using different character sets and word lengths, it may be convenient to express the capacity in equivalent bits, which is the number obtained by taking the logarithm to the base 2 of the number of usable distinguishable states in which the storage can exist. (3) The storage (or memory) capacity of a computer usually refers only to the internal storage section. 235

storage cell (secondary cell or accumulator) (1) (electric energy). A galvanic cell for the generation of electric energy in which the cell, after being discharged, may be restored to a fully charged condition by an electric current flowing in a direction opposite to the flow of current when the cell discharges. *See:* **electrochemistry.** 328

transadmittance, forward (electron tubes). The complex quotient of (1) the fundamental component of the short-circuit current induced in the second of any two gaps and (2) the fundamental component of the voltage across the first. 125

trans-μ-factor (multibeam electron tubes). The ratio of (1) the magnitude of an infinitesimal change in the voltage at the control grid of any one beam to (2) the magnitude of an infinitesimal change in the voltage at the control grid of a second beam. The current in the second beam and the voltage of all other electrodes are maintained constant. 125

transceiver (1)(data transmission). The combination of radio transmitting and receiving equipment in a common housing, usually for portable or mobile use, and employing common circuit components for both transmitting and receiving. 59

(2)(navigation aid terms). A combination transmitter and receiver in a single housing, with some components being used by both parts. *See:* **transponder.** 526

transconductance. The real part of the transadmittance. *Note:* Transconductance is, as most commonly used, the interelectrode transconductance between the control grid and the plate. At low frequencies, transconductance is the slope of the control-grid-to-plate transfer characteristic. *See:* **electron-tube admittances; interelectrode transconductance.** 125

transconductance meter (mutual-conductance meter). An instrument for indicating the transconductance of a grid-controlled electron tube. *See:* **instrument.** 328

transcribe (electronic computation). To convert data recorded in a given medium to the medium used by a digital computing machine or vice versa. 235

transcriber (electronic computation). Equipment associated with a computing machine for the purpose of transferring input (or output) data from a record of information in a given language to the medium and the language used by a digital computing machine (or from a computing machine to a record of information). 210

transducer (1)(electrical heating applications to melting furnaces and forehearths in the glass industry). A device that is actuated by power from one system and supplies power in any other form to a second system. 520

(2) (communication and power transmission). A device by means of which energy can flow from one or more transmission systems or media to one or more other transmission systems or media. *Note:* The energy transmitted by these systems or media may be of any form (for example, it may be electric, mechanical, or acoustical), and it may be of the same form or different forms in the various input and output systems or media. 111,255,54

(3) (metering). A device to receive energy from one system and supply energy, of either the same or of a different kind, to another system, in such a manner that the desired characteristics of the energy input appear at the output. 212

(4) (thyristor). A device which under the influence of a change in energy level of one form or in one system, produces a specified change in energy level of another form or in another system. 445

transducer, active. A transducer whose output waves are dependent upon sources of power, apart from that supplied by any of the actuating waves, which power is controlled by one or more of the waves. *Note:* The definition of active transducer is a restriction of the more general **active network:** that is, one in which there is an impressed driving force. *See:* **transducer.** 210

transducer gain (1) (general). The ratio of the power that the transducer delivers to the specified load under specified operating conditions to the available power of the specified source. *Notes:* (A) If the input and/or output power consist of more than one component, such as multifrequency signals or noise, then the particular components used and their weighting must be specified. (B) This gain is usually expressed in decibels. *See:* **transducer.** 210

(2) (two-port linear transducer). At a specified frequency, the ratio of (A) the actual signal power transferred from the output port of the transducer to its load, to (B) the available signal power from the source driving the transducer. 125

transducer, ideal (for connecting a specified source to a specified load). A hypothetical passive transducer that transfers the maximum available power from the source to the load. *Note:* In linear transducers having only one input and one output, and for which the impedance concept applies, this is equivalent to a transducer that (1) dissipates no energy and (2) when connected to the specified source and load presents to each its conjugate impedance. *See:* **transducer.** 210

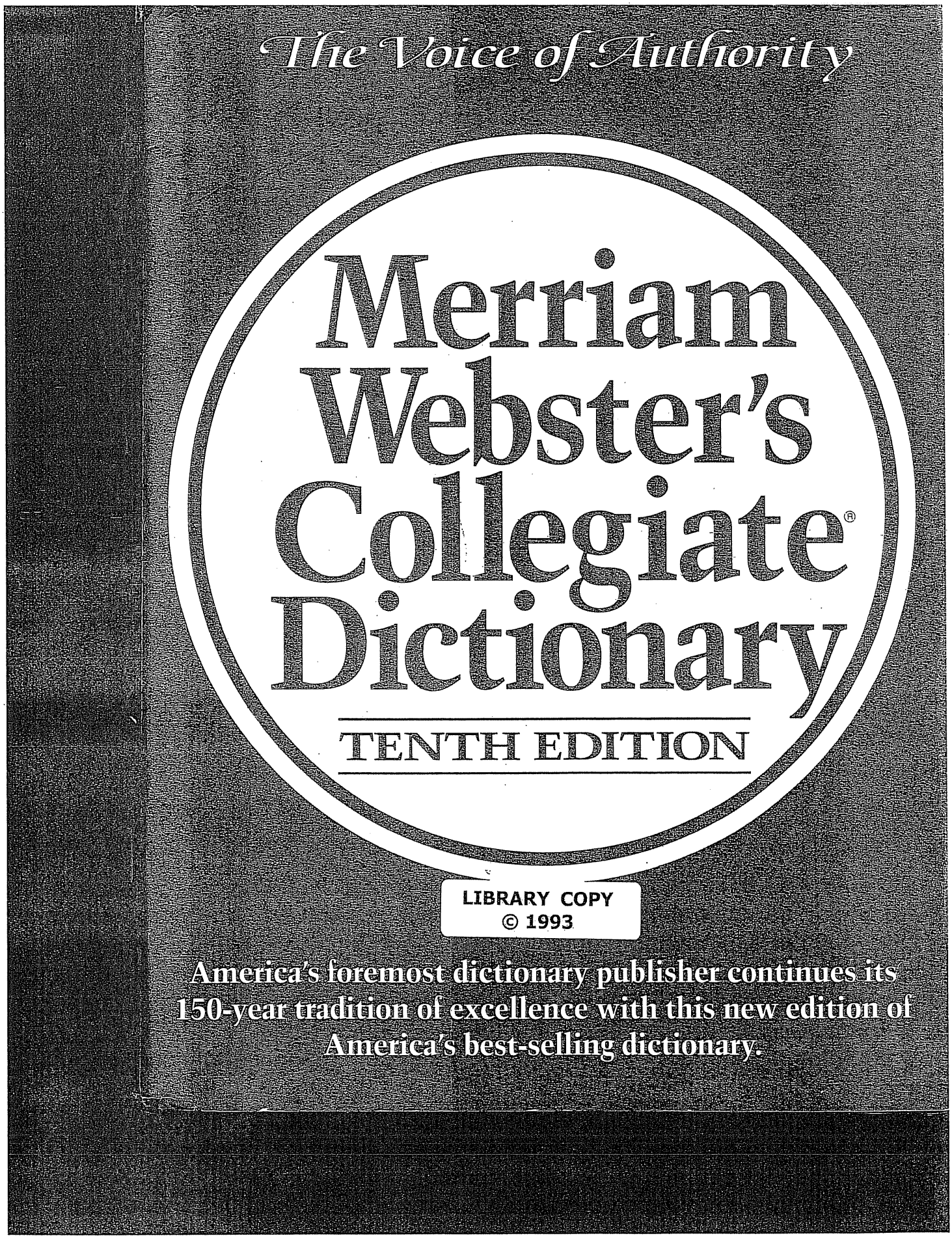
transducer, line. *See:* **line transducer.**

transducer loss. The ratio of the available power of the specified source to the power that the transducer delivers to the specified load under specified operating conditions. *Notes:* (1) If the input and/or output power consist of more than one component, such as multifrequency signals or noise, then the particular components used and their weighting must be specified. (2) This loss is usually expressed in decibels. *See:* **transducer.** 210

transducer, passive. A transducer that has no source of power other than the input signal(s), and whose output signal-power cannot exceed that of the input. *Note:* The definition of a passive transducer is a restriction of the more general **passive network,** that is, one containing no impressed driving forces. *See:* **transducer.** 210

transfer (1) (telephone switching systems). A feature that allows a customer to instruct the switching equipment or operator to transfer his call to another station. 55

(2) (electronic computation). (A) To transmit, or copy, information from one device to another. (B) To jump. (C) The act of transferring. *See:* **jump; transmit.** 235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solemn or important : POMPOUS **c** : ponderously excessive ⟨that discipline's overwrought, ~ phrases —R. M. Coles⟩ ***syn*** see OMINOUS — **por·ten·tous·ly** *adv* — **por·ten·tous·ness** *n*

[1]por·ter \'pōr-tər, 'pȯr-\ *n* [ME, fr. OF *portier*, fr. LL *portarius*, fr. L *porta* gate — more at PORT] (13c) *chiefly Brit* : a person stationed at a door or gate to admit or assist those entering

[2]porter *n* [ME *portour*, fr. MF *porteour*, fr. LL *portator*, fr. L *portare* to carry — more at FARE] (14c) **1** : a person who carries burdens; *esp* : one employed to carry baggage for patrons at a hotel or transportation terminal **2** : a parlor-car or sleeping-car attendant who waits on passengers and makes up berths **3** [short for *porter's beer*] : a heavy dark brown beer brewed from browned or charred malt **4** : a person who does routine cleaning (as in a hospital or office)

[3]porter *vt* (1609) : to transport or carry as or as if by a porter ~ *vi* : to act as a porter

por·ter·age \-tə-rij\ *n* (15c) : a porter's work; *also* : the charge for it

por·ter·house \'pōr-tər-ˌhaus, 'pȯr-\ *n* (ca. 1758) **1** *archaic* : a house where malt liquor (as porter) is sold **2** : a large steak cut from the thick end of the short loin to contain a T-shaped bone and a large piece of tenderloin — see BEEF illustration

port·fo·lio \pōrt-'fō-lē-ˌō, pȯrt-\ *n, pl* **-li·os** [It *portafoglio*, fr. *portare* to carry (fr. L) + *foglio* leaf, sheet, fr. L *folium* — more at BLADE] (1722) **1** : a hinged cover or flexible case for carrying loose papers, pictures, or pamphlets **2** [fr. the use of such a case to carry documents of state] : the office and functions of a minister of state or member of a cabinet **3** : the securities held by an investor : the commercial paper held by a financial house (as a bank) **4** : a set of pictures (as drawings or photographs) either bound in book form or loose in a folder

port·hole \'pōrt-ˌhōl, 'pȯrt-\ *n* [*2port*] (ca. 1591) **1** : an opening (as a window) with a cover or closure esp. in the side of a ship or aircraft **2** : a port through which to shoot **3** : [2]PORT 2

Por·tia \'pōr-shə, 'pȯr-\ *n* : the heroine in Shakespeare's *The Merchant of Venice*

por·ti·co \'pōr-ti-ˌkō, 'pȯr-\ *n, pl* **-coes** *or* **-cos** [It, fr. L *porticus* — more at PORCH] (1605) : a colonnade or covered ambulatory esp. in classical architecture and often at the entrance of a building

por·tiere \pōr-'tyer, pȯr-, -'tir; 'pōr-tē-ər, 'pȯr-\ *n* [F *portière*, fr. OF, fem. of *portier* porter, doorkeeper] (1843) : a curtain hanging across a doorway

[1]por·tion \'pōr-shən, 'pȯr-\ *n* [ME, fr. OF, fr. L *portion-, portio;* akin to L *part-, pars* part] (14c) **1** : an individual's part or share of something: as **a** : a share received by gift or inheritance **b** : DOWRY **c** : a helping of food **2** : an individual's lot, fate, or fortune : one's share of good and evil **3** : an often limited part set off or abstracted from a whole ⟨give but that ~ which yourself proposed —Shak.⟩ ***syn*** see PART, FATE

[2]portion *vt* **por·tioned; por·tion·ing** \-sh(ə-)niŋ\ (14c) **1** : to divide into portions : DISTRIBUTE **2** : to allot a dowry to : DOWER

por·tion·less \-shən-ləs\ *adj* (1782) : having no portion; *esp* : having no dowry or inheritance

port·land cement \'pōrt-lən(d)-, 'pȯrt-\ *n* [Isle of *Portland*, England; fr. its resemblance to a limestone found there] (1824) : a hydraulic cement made by finely pulverizing the clinker produced by calcining to incipient fusion a mixture of clay and limestone or similar materials

port·ly \'pōrt-lē, 'pȯrt-\ *adj* **port·li·er; -est** [*3port*] (15c) **1** : DIGNIFIED, STATELY **2** : heavy or rotund of body : STOUT — **port·li·ness** *n*

[1]port·man·teau \pōrt-'man-(ˌ)tō, pȯrt-\ *n, pl* **-teaus** *or* **-teaux** \-(ˌ)tōz\ [MF *portemanteau*, fr. *porter* to carry + *manteau* mantle, fr. L *mantellum* — more at PORT] (1579) **1** : a large suitcase **2** : a word or morpheme whose form and meaning are derived from a blending of two or more distinct forms (as *smog* from *smoke* and *fog*)

[2]portmanteau *adj* (1909) **1** : combining more than one use or quality **2** : being a portmanteau ⟨a ~ word⟩

port of call (1884) **1** : an intermediate port where ships customarily stop for supplies, repairs, or transshipment of cargo **2** : a stop included on an itinerary

port of entry (1840) **1** : a place where foreign goods may be cleared through a customhouse **2** : a place where an alien may be permitted to enter a country

por·trait \'pōr-trət, 'pȯr-, -ˌtrāt\ *n* [MF, fr. pp. of *portraire*] (1570) **1** : PICTURE; *esp* : a pictorial representation (as a painting) of a person usu. showing the face **2** : a sculptured figure : BUST, STATUE **3** : a graphic portrayal in words

por·trait·ist \-trə-tist, -ˌtrā-\ *n* (1866) : a maker of portraits

por·trai·ture \'pōr-trə-ˌchůr, 'pȯr-, -chər, -ˌtyůr, -ˌtůr\ *n* (14c) **1** : the making of portraits : PORTRAYAL **2** : PORTRAIT

por·tray \pōr-'trā, pȯr-, pər-\ *vt* [ME *portraien*, fr. MF *portraire*, fr. L *protrahere* to draw forth, reveal, expose — more at PROTRACT] (14c) **1** : to make a picture of : DEPICT **2** **a** : to describe in words **b** : to play the role of : ENACT — **por·tray·er** *n*

por·tray·al \-'trā(-ə)l\ *n* (ca. 1847) **1** : the act or process or an instance of portraying : REPRESENTATION **2** : PORTRAIT

por·tress \'pōr-trəs, 'pȯr-\ *n* (15c) : a female porter: as **a** : a doorkeeper in a convent or apartment house **b** : CHARWOMAN

Port Roy·al·ist \pōrt-'rȯi-ə-list, pȯrt-\ *n* [F *portroyaliste*, fr. *Port-Royal*, a convent near Versailles, France] (ca. 1741) : a member or adherent of a 17th century French Jansenist lay community noted for its logicians and educators

Port Sa·lut \ˌpȯr-sə-'lü, -sa-; -səl-'yü, -sal-\ *n* (1902) : PORT DU SALUT

Por·tu·guese \'pōr-chə-ˌgēz, 'pȯr-, -ˌgēs; ˌpōr-chə-', ˌpȯr-\ *n, pl* **Portuguese** [Pg *português*, adj. & n., fr. *Portugal*] (1534) **1** **a** : a native or inhabitant of Portugal **b** : one who is of Portuguese descent **2** : the Romance language of Portugal and Brazil — **Portuguese** *adj*

Portuguese man–of–war *n, pl* **Portuguese man–of–wars** *also* **Portuguese men–of–war** (1707) : any of a genus (*Physalia*) of large tropical and subtropical pelagic siphonophores having a crested bladderlike float which bears the colony comprised of three types of zooids on the lower surface with one of the three having nematocyst-equipped tentacles

Portuguese man-of-war

por·tu·laca \ˌpōr-chə-'la-kə, ˌpȯr-\ *n* [NL, fr. L, purslane, fr. *portula*, dim. of *porta* gate; fr. the lid of its capsule — more at PORT] (1548) : any of a genus (*Portulaca*) of mainly tropical succulent herbs of the purslane family; *esp* : a widely cultivated plant (*P. grandiflora*) with showy flowers and small conical leaves

port–wine stain \'pōrt-'wīn-, 'pȯrt-\ *n* (ca. 1909) : a reddish purple superficial hemangioma of the skin commonly occurring as a birthmark

po·sa·da \pə-'sä-də\ *n* [Sp, fr. *posar* to lodge, fr. LL *pausare*] (1763) : an inn in Spanish-speaking countries

[1]pose \'pōz\ *vb* **posed; pos·ing** [ME, fr. MF *poser*, fr. (assumed) VL *pausare*, fr. LL, to stop, rest, pause, fr. L *pausa* pause] *vt* (14c) **1** **a** : to present for attention or consideration ⟨let me ~ a question⟩ **b** : to put or set forth : OFFER ⟨this attitude ~s a threat to our hopes for peace⟩ **2** **a** : to put or set in place **b** : to place (as a model) in a studied attitude ~ *vi* **1** : to assume a posture or attitude usu. for artistic purposes **2** : to affect an attitude or character usu. to deceive or impress

[2]pose *n* (1818) **1** : a sustained posture; *esp* : one assumed for artistic effect **2** : an attitude, role, or characteristic assumed for effect
syn POSE, AIR, AIRS, AFFECTATION, MANNERISM mean an adopted way of speaking or behaving. POSE implies an attitude deliberately assumed in order to impress others ⟨her shyness was just a *pose*⟩. AIR may suggest natural acquirement through environment or way of life ⟨a traveler's sophisticated *air*⟩. AIRS always implies artificiality and pretentiousness ⟨snobbish *airs*⟩. AFFECTATION applies to a trick of speech or behavior that strikes the observer as insincere ⟨the posh accent is an *affectation*⟩. MANNERISM applies to an acquired eccentricity that has become a habit ⟨gesturing with a cigarette was her most noticeable *mannerism*⟩.

[3]pose *vt* **posed; pos·ing** [short for earlier *appose*, fr. ME *apposen*, alter. of *opposen* to oppose] (1593) : PUZZLE, BAFFLE

Po·sei·don \pə-'sī-dᵊn\ *n* [L, fr. Gk *Poseidōn*] : the Greek god of the sea — compare NEPTUNE

[1]pos·er \'pō-zər\ *n* [*3pose*] (1793) : a puzzling or baffling question

[2]poser *n* [*1pose*] (1888) : a person who poses

po·seur \pō-'zər\ *n* [F, lit., poser, fr. *poser*] (1872) : a person who pretends to be what he or she is not : an affected or insincere person

posh \'päsh\ *adj* [origin unknown] (1918) : ELEGANT, FASHIONABLE — **posh·ly** *adv* — **posh·ness** *n*

pos·it \'pä-zət\ *vt* **pos·it·ed** \'pä-zə-təd, 'päz-təd\; **pos·it·ing** \'pä-zə-tiŋ, 'päz-tiŋ\ [L *positus*, pp. of *ponere*] (1647) **1** : to dispose or set firmly : FIX **2** : to assume or affirm the existence of : POSTULATE **3** : to propose as an explanation : SUGGEST

[1]po·si·tion \pə-'zi-shən\ *n* [ME *posycion*, fr. MF *position*, fr. L *position-, positio*, fr. *ponere* to lay down, put, place, fr. (assumed) OL *posinere*, fr. *po-* away (akin to OCS *po-*, perfective prefix, Gk *apo* away) + L *sinere* to leave — more at OF] (14c) **1** : an act of placing or arranging: as **a** : the laying down of a proposition or thesis **b** : an arranging in order **2** : a point of view adopted and held to ⟨made my ~ on the issue clear⟩ **3** **a** : the point or area occupied by a physical object ⟨took her ~ at the head of the line⟩ **b** : a certain arrangement of bodily parts ⟨rose to a standing ~⟩ **4** : a market commitment in securities or commodities; *also* : the inventory of a market trader **5** **a** : relative place, situation, or standing ⟨is now in a ~ to make decisions on his own⟩ **b** : social or official rank or status **c** : an employment for which one has been hired : JOB ⟨a ~ with a brokerage firm⟩ **d** : a situation that confers advantage or preference

[2]position *vt* **po·si·tioned; po·si·tion·ing** \pə-'zi-sh(ə-)niŋ\ (1817) : to put in proper position; *also* : LOCATE

po·si·tion·al \pə-'zi-sh(ə-)nəl\ *adj* (1571) **1** : of, relating to, or fixed by position ⟨~ astronomy⟩ **2** : involving little movement ⟨~ warfare⟩ **3** : dependent on position or environment or context ⟨the front-articulated \k\ in \kē\ *key* and the back-articulated \k\ in \kül\ *cool* are ~ variants⟩ — **po·si·tion·al·ly** *adv*

positional notation *n* (1941) : a system of expressing numbers in which the digits are arranged in succession, the position of each digit has a place value, and the number is equal to the sum of the products of each digit by its place value

position effect *n* (1930) : genetic effect that is due to interaction of adjacent genes and that is modified when the spatial relationships of the genes change (as by chromosomal inversion)

position paper *n* (1949) : a detailed report that recommends a course of action on a particular issue

[1]pos·i·tive \'pä-zə-tiv, 'päz-tiv\ *adj* [ME, fr. MF *positif*, fr. L *positivus*, fr. *positus*, pp. of *ponere*] (14c) **1** **a** : formally laid down or imposed : PRESCRIBED ⟨~ laws⟩ **b** : expressed clearly or peremptorily ⟨her answer was a ~ *no*⟩ **c** : fully assured : CONFIDENT **2** **a** : of, relating to, or constituting the degree of comparison that is expressed in English by the unmodified and uninflected form of an adjective or adverb and denotes no increase or diminution **b** (1) : independent of changing circumstances : UNCONDITIONED (2) : relating to or constituting a motion or device that is definite, unyielding, constant, or certain in its action ⟨a ~ system of levers⟩ **c** (1) : INCONTESTABLE ⟨~ proof⟩ (2) : UNQUALIFIED ⟨a ~ disgrace⟩ **3** **a** : not fictitious : REAL ⟨a ~ influence for good in the community⟩ **b** : active and effective in social or economic function rather than merely maintaining peace and order ⟨a ~ government⟩ **4** **a** : having or expressing actual existence or quality as distinguished from deprivation or deficiency ⟨~ change in temperature⟩: as (1) : capable of being constructively applied (2) : not speculative : EMPIRICAL **b** : having rendition of light and shade similar in tone to the tones of the original subject ⟨a ~ photographic image⟩ **c** : that is or is generated in a direction arbitrarily or customarily taken as that of increase or progression ⟨~ rotation of the earth⟩ ⟨we are making some ~ progress⟩ **d** : directed or moving toward a source of stimulation ⟨a ~ taxis⟩ **e** : real and numerically greater than zero ⟨+2 is a ~ integer⟩ **5** **a** (1) : being, relating to, or charged with electricity of which the proton is the elementary unit and which predominates in a glass body after being rubbed with silk (2) : having more protons than electrons ⟨a ~ ion⟩ **b** (1) : having higher electric potential and constituting the part from which the current flows to the external circuit ⟨the ~ terminal of a discharging storage battery⟩ (2) : being an electron-collecting electrode of an electron tube **6** **a**

trans·at·lan·tic \ˌtran(t)s-ət-'lan-tik, ˌtranz-\ *adj* (1779) 1 a : crossing or extending across the Atlantic Ocean ⟨a ~ cable⟩ b : relating to or involving crossing the Atlantic Ocean ⟨~ air fares⟩ 2 a : situated or originating from beyond the Atlantic Ocean b : of, relating to, or involving countries on both sides of the Atlantic Ocean and esp. the U.S. and Great Britain ⟨~ cooperation⟩

trans·ax·le \tran(t)s-'ak-səl, tranz-\ *n* [*trans*mission + *axle*] (1958) : a unit that consists of a combination of transmission and front axle used in front-wheel-drive automobiles

trans·ceiv·er \tran(t)-'sē-vər\ *n* [*trans*mitter + *receiver*] (1934) : a radio transmitter-receiver that uses many of the same components for both transmission and reception

tran·scend \tran(t)-'send\ *vb* [ME, fr. L *transcendere* to climb across, transcend, fr. *trans-* + *scandere* to climb — more at SCAN] *vt* (14c) 1 a : to rise above or go beyond the limits of b : to triumph over the negative or restrictive aspects of : OVERCOME c : to be prior to, beyond, and above (the universe or material existence) 2 : to outstrip or outdo in some attribute, quality, or power ~ *vi* : to rise above or extend notably beyond ordinary limits *syn* see EXCEED

tran·scen·dence \-'sen-dən(t)s\ *n* (1601) : the quality or state of being transcendent

tran·scen·den·cy \-dən(t)-sē\ *n* (1615) : TRANSCENDENCE

tran·scen·dent \-dənt\ *adj* [L *transcendent-, transcendens*, prp. of *transcendere*] (1598) 1 a : exceeding usual limits : SURPASSING b : extending or lying beyond the limits of ordinary experience c *in Kantian philosophy* : being beyond the limits of all possible experience and knowledge 2 : being beyond comprehension 3 : transcending the universe or material existence — **tran·scen·dent·ly** *adv*

tran·scen·den·tal \ˌtran(t)-ˌsen-'den-tᵊl, -sən-\ *adj* (1624) 1 a : TRANSCENDENT 1b b : SUPERNATURAL c : ABSTRUSE, ABSTRACT d : of or relating to transcendentalism 2 a : incapable of being the root of an algebraic equation with rational coefficients ⟨π is a ~ number⟩ b : being, involving, or representing a function (as sin x, log x, e^x) that cannot be expressed by a finite number of algebraic operations ⟨~ curves⟩ 3 *in Kantian philosophy* a : of or relating to experience as determined by the mind's makeup b : transcending experience but not human knowledge 4 : TRANSCENDENT 1a — **tran·scen·den·tal·ly** \-tᵊl-ē\ *adv*

tran·scen·den·tal·ism \-tᵊl-ˌi-zəm\ *n* (1803) 1 : a philosophy that emphasizes the a priori conditions of knowledge and experience or the unknowable character of ultimate reality or that emphasizes the transcendent as the fundamental reality 2 : a philosophy that asserts the primacy of the spiritual and transcendental over the material and empirical 3 : the quality or state of being transcendental; *esp* : visionary idealism — **tran·scen·den·tal·ist** \-tᵊl-ist\ *adj or n*

transcendental meditation *n* (1966) : a technique of meditation in which a mantra is chanted in order to foster calm, creativity, and spiritual well-being

trans·con·ti·nen·tal \ˌtran(t)s-ˌkän-tᵊn-'en-tᵊl, ˌtranz-\ *adj* (1853) : extending or going across a continent ⟨a ~ railroad⟩

tran·scribe \tran(t)-'skrīb\ *vt* **tran·scribed; tran·scrib·ing** [L *transcribere*, fr. *trans-* + *scribere* to write — more at SCRIBE] (1552) 1 a : to make a written copy of b : to make a copy of (dictated or recorded matter) in longhand or on a machine (as a typewriter) c : to paraphrase or summarize in writing d : WRITE DOWN, RECORD 2 a : to represent (speech sounds) by means of phonetic symbols b : TRANSLATE 2a c : to transfer (data) from one recording form to another d : to record (as on magnetic tape) for later broadcast 3 : to make a musical transcription of 4 : to cause (as DNA) to undergo genetic transcription — **tran·scrib·er** *n*

tran·script \'tran(t)-ˌskript\ *n* [ME, fr. ML *transcriptum*, fr. L, neut. of *transcriptus*, pp. of *transcribere*] (14c) 1 a : a written, printed, or typed copy; *esp* : a usu. typewritten copy of dictated or recorded material b : an official or legal and often published copy ⟨a court reporter's ~⟩; *esp* : an official copy of a student's educational record 2 : a representation (as of experience) in an art form 3 : a sequence of RNA produced by transcription from a DNA template

tran·scrip·tase \tran-'skrip-ˌtās, -ˌtāz\ *n* [*transcription* + *-ase*] (1963) : RNA POLYMERASE; *also* : REVERSE TRANSCRIPTASE

tran·scrip·tion \tran(t)-'skrip-shən\ *n* (1598) 1 : an act, process, or instance of transcribing 2 : COPY, TRANSCRIPT; as a : an arrangement of a musical composition for some instrument or voice other than the original b : a recording (as on magnetic tape) made esp. for use in radiobroadcasting 3 : the process of constructing a messenger RNA molecule using a DNA molecule as a template with resulting transfer of genetic information to the messenger RNA — compare TRANSLATION 2, REVERSE TRANSCRIPTION — **tran·scrip·tion·al** \-shnəl, -shə-nᵊl\ *adj* — **tran·scrip·tion·al·ly** *adv*

tran·scrip·tion·ist \-shə-nist\ *n* (1963) : one that transcribes; *esp* : a typist who transcribes dictated medical reports

trans·cul·tur·al \tran(t)s-'kəl-chə-rəl, tranz-, -'kəlch-rəl\ *adj* (1951) : involving, encompassing, or extending across two or more cultures ⟨~ problems⟩

trans·cu·ta·ne·ous \ˌtran(t)s-kyü-'tā-nē-əs\ *adj* (ca. 1941) : passing, entering, or made by penetration through the skin ⟨~ infection⟩ ⟨~ inoculation⟩

trans·der·mal \tran(t)s-'dər-məl, tranz-\ *adj* (1944) : relating to, being, or supplying a medication in a form for absorption through the skin into the bloodstream ⟨~ drug delivery⟩ ⟨~ nitroglycerin⟩ ⟨~ nicotine patch⟩

trans·dis·ci·plin·ary \-'di-sə-plə-ˌner-ē\ *adj* (1948) : INTERDISCIPLINARY

trans·duce \tran(t)s-'düs, tranz-, -'dyüs\ *vt* **trans·duced; trans·duc·ing** [L *transducere* to lead across, transfer, fr. *trans-* + *ducere* to lead — more at TOW] (1947) 1 : to convert (as energy or a message) into another form ⟨essentially sense organs ~ physical energy into a nervous signal⟩ 2 : to bring about the transfer of (as a gene) from one microorganism to another by means of a viral agent

trans·duc·er \-'dü-sər, -'dyü-\ *n* (1924) : a device that is actuated by power from one system and supplies power usu. in another form to a second system ⟨a loudspeaker is a ~ that transforms electrical signals into sound energy⟩

trans·duc·tion \-'dək-shən\ *n* [L *transducere*] (1947) : the action or process of transducing; *esp* : the transfer of genetic determinants from one microorganism to another by a viral agent (as a bacteriophage) — **trans·duc·tant** \-tənt\ *n* — **trans·duc·tion·al** \-shnəl, -shə-nᵊl\ *adj*

¹tran·sect \tran(t)-'sekt\ *vt* [*trans-* + *intersect*] (1634) : to cut transversely — **tran·sec·tion** \-'sek-shən\ *n*

²tran·sect \'tran(t)-ˌsekt\ *n* (1905) : a sample area (as of vegetation) usu. in the form of a long continuous strip

tran·sept \'tran(t)-ˌsept\ *n* [NL *transeptum*, fr. L *trans-* + *septum*, *saeptum* enclosure, wall] (ca. 1542) : the part of a cruciform church that crosses at right angles to the greatest length between the nave and the apse or choir; *also* : either of the projecting ends of a transept — **tran·sep·tal** \tran(t)-'sep-tᵊl\ *adj*

trans·fec·tion \tran(t)s-'fek-shən, tranz-\ *n* [*trans-* + in*fection*] (1964) : infection of a cell with isolated viral nucleic acid followed by production of the complete virus in the cell; *also* : the incorporation of exogenous DNA into a cell — **trans·fect** \-'fekt\ *vt*

¹trans·fer \tran(t)s-'fər, 'tran(t)s-ˌ\ *vb* **trans·ferred; trans·fer·ring** [ME *transferren*, fr. L *transferre*, fr. *trans-* + *ferre* to carry — more at BEAR] *vt* (14c) 1 a : to convey from one person, place, or situation to another : TRANSPORT b : to cause to pass from one to another : TRANSMIT c : TRANSFORM, CHANGE 2 : to make over the possession or control of : CONVEY 3 : to print or otherwise copy from one surface to another by contact ~ *vi* 1 : to move to a different place, region, or situation; *esp* : to withdraw from one educational institution to enroll at another 2 : to change from one vehicle or transportation line to another — **trans·fer·abil·i·ty** \(ˌ)tran(t)s-ˌfər-ə-'bi-lə-tē\ *n* — **trans·fer·able** *also* **trans·fer·ra·ble** \tran(t)s-'fər-ə-bəl\ *adj* — **trans·fer·al** \-əl\ *n* — **trans·fer·rer** \-ər\ *n*

²trans·fer \'tran(t)s-ˌfər\ *n* (1674) 1 a : conveyance of right, title, or interest in real or personal property from one person to another b : removal or acquisition of property by mere delivery with intent to transfer title 2 a : an act, process, or instance of transferring : TRANSFERENCE 2 b : the carryover or generalization of learned responses from one type of situation to another 3 : one that transfers or is transferred; *esp* : a graphic image transferred by contact from one surface to another 4 : a place where a transfer is made (as of trains to ferries or as where one form of power is changed to another) 5 : a ticket entitling a passenger on a public conveyance to continue the trip on another route

trans·fer·ase \'tran(t)s-(ˌ)fər-ˌās, -ˌāz\ *n* (1948) : an enzyme that promotes transfer of a group from one molecule to another

trans·fer·ee \ˌtran(t)s-(ˌ)fər-'ē\ *n* (ca. 1736) 1 : a person to whom a conveyance is made 2 : one who is transferred

trans·fer·ence \tran(t)s-'fər-ən(t)s, 'tran(t)s-(ˌ)\ *n* (1681) 1 : an act, process, or instance of transferring : CONVEYANCE, TRANSFER 2 : the redirection of feelings and desires and esp. of those unconsciously retained from childhood toward a new object (as a psychoanalyst conducting therapy) — **trans·fer·en·tial** \ˌtran(t)s-fə-'ren(t)-shəl\ *adj*

transfer factor *n* (1956) : a substance that is produced and secreted by a lymphocyte functioning in cell-mediated immunity and that upon incorporation into a lymphocyte which has not been sensitized confers on it the same immunological specificity as the sensitized cell

trans·fer·or \ˌtran(t)s-(ˌ)fər-'ȯr\ *n* (1875) : one that conveys a title, right, or property

transfer payment *n* (ca. 1945) 1 : a public expenditure made for a purpose (as unemployment compensation) other than procuring goods or services — usu. used in pl. 2 *pl* : money (as welfare payments) that is received by individuals and that is neither compensation for goods or services currently supplied nor income from investments

trans·fer·rin \tran(t)s-'fer-ən\ *n* [*trans-* + L *ferrum* iron] (1947) : a beta globulin in blood plasma capable of combining with ferric ions and transporting iron in the body

transfer RNA \'tran(t)s-ˌfər-\ *n* (1961) : a relatively small RNA that transfers a particular amino acid to a growing polypeptide chain at the ribosomal site of protein synthesis during translation — compare MESSENGER RNA

trans·fig·u·ra·tion \(ˌ)tran(t)s-ˌfi-gyə-'rā-shən, -gə-\ *n* (14c) 1 a : a change in form or appearance : METAMORPHOSIS b : an exalting, glorifying, or spiritual change 2 *cap* : August 6 observed as a Christian feast in commemoration of the transfiguration of Christ on a mountaintop in the presence of three disciples

trans·fig·ure \tran(t)s-'fi-gyər, *esp Brit* -'fig-ər\ *vt* **-ured; -ur·ing** [ME, fr. L *transfigurare*, fr. *trans-* + *figurare* to shape, fashion, fr. *figura* figure] (14c) : to give a new and typically exalted or spiritual appearance to : transform outwardly and usu. for the better *syn* see TRANSFORM

trans·fi·nite \(ˌ)tran(t)s-'fī-ˌnīt\ *adj* [G *transfinit*, fr. *trans-* (fr. L) + *finit* finite, fr. L *finitus*] (1902) 1 : going beyond or surpassing any finite number, group, or magnitude 2 : being or relating to cardinal and ordinal numbers of sets with an infinite number of elements

trans·fix \tran(t)s-'fiks\ *vt* [L *transfixus*, pp. of *transfigere*, fr. *trans-* + *figere* to fasten, pierce — more at FIX] (1590) 1 : to pierce through with or as if with a pointed weapon : IMPALE 2 : to hold motionless by or as if by piercing — **trans·fix·ion** \-'fik-shən\ *n*

¹trans·form \tran(t)s-'fȯrm\ *vb* [ME, fr. L *transformare*, fr. *trans-* + *formare* to form, fr. *forma* form] *vt* (14c) 1 a : to change in composition or structure b : to change the outward form or appearance of c : to change in character or condition : CONVERT 2 : to subject to mathematical transformation 3 : to cause (a cell) to undergo genetic transformation ~ *vi* : to become transformed : CHANGE — **trans·form·able** \-'fȯr-mə-bəl\ *adj* — **trans·for·ma·tive** \-'fȯr-mə-tiv\ *adj*

syn TRANSFORM, METAMORPHOSE, TRANSMUTE, CONVERT, TRANSMOGRIFY, TRANSFIGURE mean to change a thing into a different thing. TRANSFORM implies a major change in form, nature, or function ⟨*transformed* a small company into a corporate giant⟩. METAMORPHOSE suggests an abrupt or startling change induced by or as if by magic or a supernatural power ⟨awkward girls *metamorphosed* into graceful ballerinas⟩. TRANSMUTE implies transforming into a higher element or thing ⟨at-

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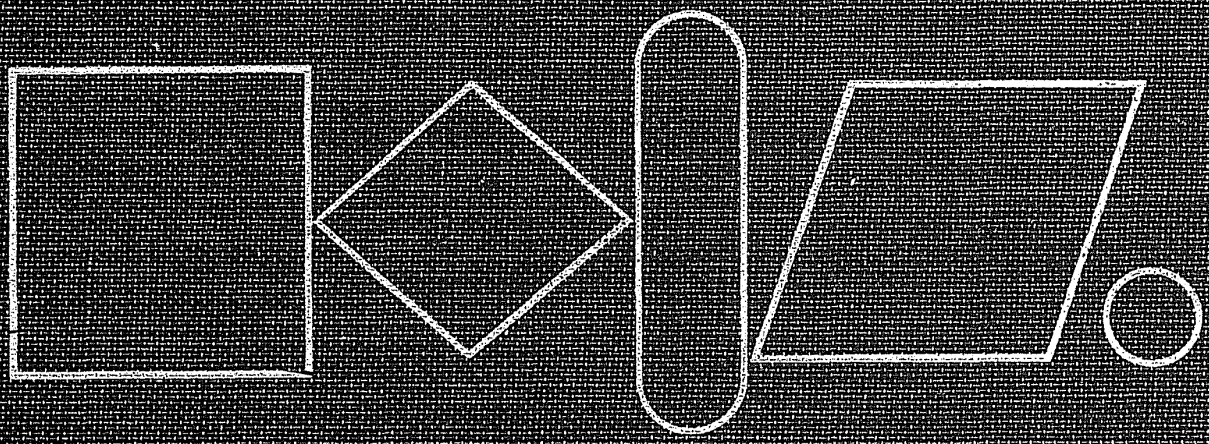


STANDARD DICTIONARY OF COMPUTERS AND INFORMATION PROCESSING

MARTIN H. WEIK

HAYDEN BOOK COMPANY, INC., NEW YORK

To my wife and children, whose patience with me was often tried during the years of preparation, and to the many wonderful friends with whom I have worked in many vocabulary efforts.

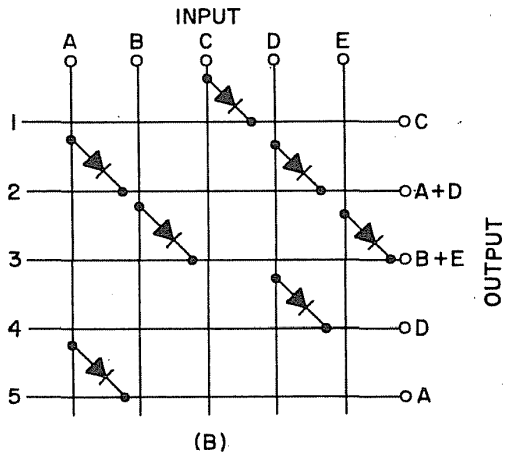
END PAPERS:
Computer tree traces growth of computers starting with the ENIAC in 1945.

Third printing, 1970

according to the manner of interconnection. The elements may be transistor, diode, or relay gates, thus performing logic functions, such as transliteration of characters, encoding, decoding, path selection, number system transformation, or word translation. Usually in a rectangular planar array, input is taken along one dimension and output is taken along the other. (Synonymous with *matrix switch.*)

a	b	c
4	e	f
e	b	3
g	8	h

(A)



(A) A matrix *of mathematical symbols, and (B) a diode* matrix *for decoding binary numerals.*

matrix, program timing—An array of connections in a synchronous digital computer which supplies timing pulses at regular intervals in proper sequence to permanently selected groups of lines, thus setting up an operation for execution. The timing pulses are also called clock pulses and the program timing matrix a clock-pulse generator.

matrix printer—See *printer, matrix.*

matrix switch—Same as *matrix (2).*

maximal—Pertaining to the most, greatest, largest, highest, longest, or similar superlative. (Contrast with *minimal.*)

MDE—An abbreviation for Magnetic Decision Element. (Further clarified by *element, logic.*)

mean-time-between-failures—The limit of the ratio of operating time of equipment to the number of observed failures as the number of failures approaches infinity. Abbreviated MTBF. (Contrast with *mean-time-to-failure.*)

mean-time-to-failure—The average or mean time between initial operation and the first occurrence of a failure or malfunction, as the number of measurements of such time on many pieces of identical equipment approaches infinity. Abbreviated MTTF. (Contrast with *mean-time-between-failures.*)

measurement, work—A method of establishing a relationship between the quantity and quality of work performed and the man and machine power utilized.

mechanical dictionary—Same as *dictionary, automatic.*

mechanical differential analyzer—See *analyzer, mechanical differential.*

mechanical replacement—See *replacement, mechanical.*

mechanical translation—See *translation, mechanical.*

mechanized—Same as *readable, machine.*

mechanized data—Same as *data, machine-readable.*

medium—A material or method for storing or otherwise handling data; for example, magnetic cores, paper tape, magnetic tape, punched cards, microfiche, laser emulsion, delay-lines, and microfilm. These data carriers provide for storage, mobility, and transportability of data. (Synonymous with *data medium.* Further clarified by *carrier, data* and by *medium, input-output.*)

medium, input-output—A material substance intended for carrying recorded data and designed to be transportable independently of the reading and writing mechanism; for example, a punched card, a magnetic card, a magnetic tape, paper tape, a paper sheet, preprinted stationery, or microfilm. The medium is handled by an input-output device, such as a card reader-punch, a magnetic tape handler, a paper tape perforator, a high-speed printer, or a camera. The medium is used to insert data and instructions into a computer and to remove results. (Further clarified by *medium* and by *carrier, data.*)

medium, machine-readable—A data medium that can be used to convey data to a sensing device; for example punched cards, punched tapes, and magnetic tapes. (Synonymous with *automated data medium* and with *mechanized data medium.*)

medium, storage—The material, or its configuration, on which data is recorded; for example, paper tape, cards, magnetic cores, magnetic tape, drums, discs, or laser-emulsion.

medium, transfer—A material that transfers a solid or liquid ink during printing, usually consisting of a sheet or ribbon of fabric, paper, or plastic film as a supporting base, with liquid or solid ink absorbed into or coated on the supporting base.

meet—Same as *AND.*

megabit—One million binary digits.

megahertz—One million cycles per second.

member, print—See *print-member.*

memory—Same as *storage.*

memory, core-rope—Same as *storage, core-rope.*

memory, Olsen—Same as *storage, core-rope.*

memory, rope—Same as *storage, core-rope.*

memory capacity—Same as *capacity, storage.*

station, way—In telegraphy, a station along a telegraph line. Signals pass into and through the way station.

stencil bit—See *bit, stencil.*

step—1: In computer programming, one operation in a routine. **2:** To cause a computer to execute one operation.

STEP—(Simple Transition to Electronic Processing). **1:** A programming technique developed by Sperry-Rand Corporation, Univac Division. **2:** (Supervisory Tape Executive Program). An executive routine for controlling data on magnetic tape on the National Cash Register NCR 304 computer. Errors during writing are detected and the data is written on another section of tape. **3:** (Standard Tape Executive Program). Same as *STEP (2).*

step, program—The execution of a single instruction, operation, or group of operations.

step, single—Pertaining to a method of operating a computer in which each operation is performed or executed in response to a single manual command.

step-by-step operation—Same as *operation, single-step.*

step change—See *change, step.*

step counter—See *counter, step.*

stepping register—Same as *register, shift.*

sticking—The tendency of a bistable device, such as a flip-flop or a switch, to remain in or switch back to a particular one of its two stable states.

stochastic—Pertaining to direct solution by trial-and-error, usually without a step-by-step approach, and involving analysis and evaluation of progress made, as in a heuristic approach to trial-and-error methods. In a stochastic approach to a problem solution, intuitive conjecture or speculation is used to select a possible solution, which is then tested against known evidence, observations or measurements. Intervening or intermediate steps toward a solution are omitted. (Contrast with *algorithm* and *heuristic.*)

stop, coded—Same as *halt, programmed.*

stop, form—A device on a machine that stops the machine when the supply of paper has run out.

stop, programmed—Same as *halt, programmed.*

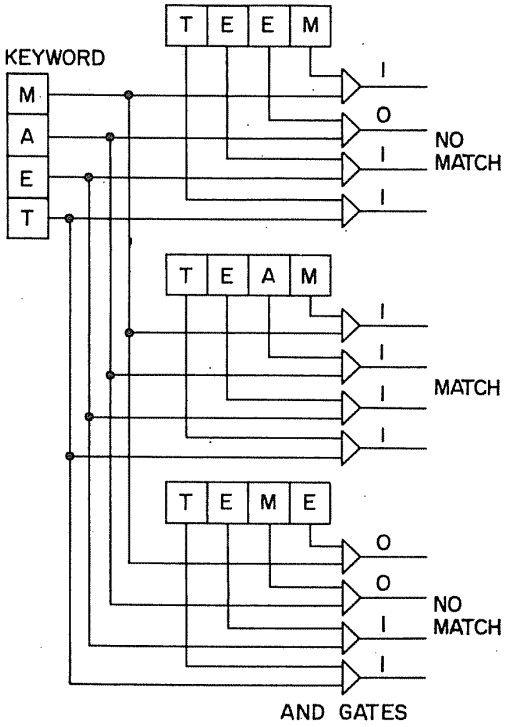
stop instruction—Same as *instruction, halt.*

stop instruction, optional—Same as *instruction, optional-halt.*

storage—A device or pertaining to a device which receives data, holds and, at a later time, returns data; for example, a plugboard, an array of magnetic cores, a magnetic disc, an electrostatic storage tube, a delay-line, or a bank of flip-flops. Various phenomena, such as electrostatic, ferroelectric, magnetic, acoustic, optical, chemical, electronic, electrical, mechanical and nuclear, are used to effect storage. (Synonymous with *store,* with *memory,* and with *computer store.*)

storage, allocate—To assign specific storage areas for specific purposes, such as holding specific routines, holding input/output data or constants, serving as working storage or scratch-pad storage, holding loading programs or executive routines, and storing priority data. (Further clarified by *allocation, storage.*)

storage, annex—Same as *storage, associative.*



All storage locations in the above associative storage *unit are queried simultaneously to determine if the given keyword is stored. If a match occurs, the appropriate storage location is identified simultaneously and immediately. Many logic elements are required.*

storage, associative—A storage device in which the storage locations are identified by their contents rather than by their names, addresses, or relative positions. The associative storage is capable of being interrogated in parallel fashion throughout its entire contents to determine whether or not a given word is stored by directly comparing it with all words stored without regard for addressing. For example, if a file consists of many sets of data elements, each element being the label for a set of allowable data items, such as the case of a personnel file, where each set of data elements pertains to a person, then each set of data elements could be put at an addressed storage location. To search for a data item as a key, such as all captains, all storage locations would have to be read and all data items compared to the key. In associative storage, a parallel-read storage operation would immediately identify and retrieve all the data items in the file that were related to the data item matching the key. In a certain sense, the search key is the address of the sought data. Thus, the associative storage quickly answers the question, "Is this word

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TQ DELTA, LLC, Plaintiff, v. COMCAST CABLE COMMUNICATIONS, LLC Defendant.	Civil Action No. 1:15-cv-00611-RGA
TQ DELTA, LLC, Plaintiff, v. COXCOM LLC and COX COMMUNICATIONS INC., Defendants.	Civil Action No. 1:15-cv-00612-RGA
TQ DELTA, LLC, Plaintiff, v. DIRECTV, LLC, Defendant.	Civil Action No. 1:15-cv-00613-RGA

TQ DELTA, LLC, Plaintiff, v. DISH NETWORK CORPORATION, DISH NETWORK LLC, DISH DBS CORPORATION, ECHOSTAR CORPORATION, and ECHOSTAR TECHNOLOGIES, LLC Defendants.	Civil Action No. 1:15-cv-00614-RGA
TQ DELTA, LLC, Plaintiff, v. TIME WARNER CABLE INC. and TIME WARNER CABLE ENTERPRISES LLC, Defendants.	Civil Action No. 1:15-cv-00615-RGA
TQ DELTA, LLC, Plaintiff, v. VERIZON SERVICES CORP., Defendant.	Civil Action No. 1:15-cv-00616-RGA

MEMORANDUM OPINION

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November 30, 2016

ANDREWS, U.S. DISTRICT JUDGE:

Presently before the Court is the issue of claim construction of multiple terms in U.S. Patent Nos. 8,718,158 ("the '158 patent"), 9,014,243 ("the '243 patent"), 8,611,404 ("the '404 patent"), 9,094,268 ("the '268 patent"), 7,835,430 ("the '430 patent"), and 8,238,412 ("the '412 patent"). The Court has considered the Parties' Joint Claim Construction Brief. (Civ. Act. No. 15-611-RGA, D.I. 144; Civ. Act. No. 15-612-RGA, D.I. 141; Civ. Act. No. 15-613-RGA, D.I. 141; Civ. Act. No. 15-614-RGA, D.I. 135; Civ. Act. No. 15-615-RGA, D.I. 141; Civ. Act. No. 15-616-RGA; D.I. 146).[1] The Court heard oral argument on October 18, 2016. (D.I. 158).

I. BACKGROUND

Plaintiff filed these actions on July 17, 2015, alleging infringement of eight patents. (D.I. 1). On July 14, 2016, Plaintiff dismissed two of these patents with prejudice. (D.I. 102). The parties divide the remaining contested patents into three groupings: the phase scrambling patents, the low power mode patents, and the diagnostic mode patents. The phase scrambling patents, which include the '158 and '243 patents, claim methods for reducing the peak to average power ratio of a multicarrier transmission system. The low power mode patents, which include the '404 and '268 patents, claim methods for causing a multicarrier communications system to enter a low power mode while storing state information for full power mode to enable a rapid start up without the need for reinitialization. The diagnostic mode patents, which include the '430 and '412 patents, claim both an apparatus and method for the reliable exchange of diagnostic and test information over a multicarrier communications system.

[1] Unless otherwise specifically noted, all references to the docket refer to Civil Action No. 15-611-RGA.

II. LEGAL STANDARD

"It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal quotation marks omitted). "'[T]here is no magic formula or catechism for conducting claim construction.' Instead, the court is free to attach the appropriate weight to appropriate sources 'in light of the statutes and policies that inform patent law.'" *SoftView LLC v. Apple Inc.*, 2013 WL 4758195, at *1 (D. Del. Sept. 4, 2013) (quoting *Phillips*, 415 F.3d at 1324) (alteration in original). When construing patent claims, a court considers the literal language of the claim, the patent specification, and the prosecution history. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 977–80 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). Of these sources, "the specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1315 (internal quotation marks omitted).

"[T]he words of a claim are generally given their ordinary and customary meaning. . . . [Which is] the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1312–13 (citations and internal quotation marks omitted). "[T]he ordinary meaning of a claim term is its meaning to [an] ordinary artisan after reading the entire patent." *Id.* at 1321 (internal quotation marks omitted). "In some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words." *Id.* at 1314.

When a court relies solely upon the intrinsic evidence—the patent claims, the specification, and the prosecution history—the court's construction is a determination of law. *See Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 841 (2015). The court may also make factual findings based upon consideration of extrinsic evidence, which "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Phillips*, 415 F.3d at 1317–19 (internal quotation marks omitted). Extrinsic evidence may assist the court in understanding the underlying technology, the meaning of terms to one skilled in the art, and how the invention works. *Id.* Extrinsic evidence, however, is less reliable and less useful in claim construction than the patent and its prosecution history. *Id.*

"A claim construction is persuasive, not because it follows a certain rule, but because it defines terms in the context of the whole patent." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998). It follows that "a claim interpretation that would exclude the inventor's device is rarely the correct interpretation." *Osram GMBH v. Int'l Trade Comm'n*, 505 F.3d 1351, 1358 (Fed. Cir. 2007) (citation and internal quotation marks omitted).

III. CONSTRUCTION OF DISPUTED TERMS

A. The Phase Scrambling Patents

The '158 patent is directed to a method for scrambling the phase characteristics of carrier signals in a multicarrier communications system. Claim 1 is representative and reads as follows:

> 1. In a *multicarrier* modulation system including a first *transceiver* in communication with a second *transceiver* using a transmission signal having a plurality of *carrier signals* for modulating a plurality of data bits, each *carrier signal* having a phase characteristic associated with at least one bit of the plurality of data bits, a method for *scrambling the phase characteristics of the carrier signals* comprising:
>
> transmitting the plurality of data bits from the first *transceiver* to the second *transceiver*;

> associating a *carrier signal* with a value determined independently of any bit of the plurality of data bits carried by the *carrier signal*, the value associated with the *carrier signal* determined by a pseudo-random number generator;
>
> *determining a phase shift for the carrier signal* at least based on the value associated with the *carrier signal*;
>
> modulating at least one bit of the plurality of data bits on the *carrier signal*;
>
> modulating the at least one bit on a second *carrier signal* of the plurality of *carrier signals*.

('158 patent, claim 1) (disputed terms italicized).

The '243 patent is also directed to a method for scrambling the phase characteristics of carrier signals in a multicarrier communications system. Claim 1 is representative and reads as follows:

> 1. A method, in a *multicarrier* communications *transceiver* comprising a *bit scrambler* followed by a *phase scrambler*, comprising:
>
> scrambling, using the *bit scrambler*, a plurality of input bits to generate a plurality of scrambled output bits, wherein at least one scrambled output bit is different than a corresponding input bit;
>
> scrambling, using the *phase scrambler*, a plurality of *carrier* phases associated with the plurality of scrambled output bits;
>
> transmitting at least one scrambled output bit on a first *carrier*; and
>
> transmitting the at least one scrambled output bit on a second *carrier*.

('243 patent, claim 1) (disputed terms italicized).

1. "carrier signal" and "carrier"

   a. *Plaintiff's proposed construction*: "plain meaning"

   b. *Defendants' proposed construction*: "wave that can be modulated to carry data"

   c. *Court's construction*: "signal that can be modulated to carry data"

The parties agree that "carrier signal" and "carrier" should have the same construction. (D.I. 144 at 36). Defendants argue strenuously that the proper construction for this term requires that the carrier signal be a wave and that this construction is supported by the specification itself. (*Id.* at 33). Contrary to Defendants' assertion, however, neither "wave" nor "waveform" appear anywhere in the specification. To require that the carrier be a wave, therefore, would be to import

a term that itself requires construction. Plaintiff argues that the wave Defendants refer to throughout their briefing and during oral argument is simply the time domain representation of a signal that exists only after the carrier signals are modulated and combined. (*Id.* at 21, 33, 35; D.I. 158 at 70:12-18). The specification supports Plaintiff's position, describing the carrier signals as being modulated in the frequency domain prior to being combined into the time domain transmission signal. ('158 patent at 4:12-24). While I find support for Plaintiff's opposition to using the word "wave" in the construction of this term, I agree with Defendants that some construction is needed, so I will adopt Defendants' construction modified as follows: "signal that can be modulated to carry data."

2. "determin[e/ing] a phase shift for the carrier signal"

   a. *Plaintiff's proposed construction*: "plain meaning"

   b. *Defendants' proposed construction*: "use/using an equation to compute the degrees or radians that the phase of the carrier signal can be shifted"

   c. *Court's construction*: "comput[e/ing] an amount by which the phase of the carrier signal will be shifted"

As an initial matter, the parties disagree as to whether the phase shift must be determined in units of degrees or radians. There is no support in the intrinsic record for Defendants' attempt to import these terms into the claim. Degrees and radians are merely units of measure, akin to feet or meters. I see no reason to limit this claim term to require specific units of measure for the phase shift.

Defendants next argue that this term should be construed to limit the meaning of "determine" to mean compute. Defendants cite the invention as described in the "Summary of the Invention" section of the specification as support and argue that the invention as a whole is described using the word "compute" with respect to how the phase shift is determined. (D.I. 144

at 38). I agree with Defendants. The specification, in describing the "present invention," states that "[a] phase shift is computed for each carrier signal." ('158 patent at 2:39-40). Every reference to the phase shift in the Summary of the Invention section reflects that the shift is "computed." *See id.* at 2:43, 2:58-59, 2:63-64. "When a patent thus describes the features of the 'present invention' as a whole, this description limits the scope of the invention." *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007).

Defendants further argue that "by definition, to 'compute' is to use an equation." (D.I. 144 at 39). Plaintiff counters that the definition of compute is broader and that Defendants are "attempting to import a limitation from an example embodiment." (*Id.* at 39-40). On this point I agree with Plaintiff. Although the example embodiments do employ an equation to compute the phase shifts, the specification disclaims reliance on any particular method, stating that "additional and/or different phase shifting techniques can be used by the phase scrambler." ('158 patent at 8:14-15). Defendants also cite to the provisional application as further support for their argument; however, the provisional application also disclaims reliance on any particular method for determining the phase shifts, stating that "[t]he fundamental principle used in this invention is to use known parameters at the transmitter and the receiver to randomize the phase of the tones in a multicarrier system." (D.I. 146 at A355).

Therefore, I decline to adopt either Plaintiff's or Defendants' proposed constructions. Instead I construe the term "determin[e/ing] a phase shift for the carrier signal" to mean "comput[e/ing] an amount by which the phase of the carrier signal will be shifted."

3. "phase scrambler"

   a. *Plaintiff's proposed construction*: "a component operable to adjust the phases of the carriers, by pseudo-randomly varying amounts"

b. *Defendants' proposed construction*: "component that adjusts the phases of modulated carrier signals by pseudo-randomly varying amounts"

c. *Court's construction*: "component operable to adjust the phases of the carrier signals, by pseudo-randomly varying amounts"

"scrambling the phase characteristics of the carrier signals"

a. *Plaintiff's proposed construction*: "adjusting the phase characteristics of the carrier signals by pseudo-randomly varying amounts"

b. *Defendants' proposed construction*: "adjusting the phases of the modulated carrier signals by pseudo-randomly varying amounts"

c. *Court's construction*: "adjusting the phase characteristics of the carrier signals by pseudo-randomly varying amounts"

The parties' only dispute with respect to these two claim terms is whether the carrier signals are modulated before or after phase scrambling occurs. Plaintiff argues that in every embodiment disclosed in the specification phase scrambling occurs before modulation. (D.I. 144 at 42). Defendants counter that the specification requires "adding phase shifts to modulated carrier signals." (*Id.* at 43). I find that Plaintiff's position is supported by the patent. For example, the specification describes the process that takes place in the transmitter as "adjusting the phase characteristic of each carrier signal and combining these carrier signals to produce the transmission signal." ('158 patent, 5:16-19). The specification also provides descriptions of several different phase shifting examples, and then states, "The DMT transmitter 22 then combines (step 130) the carrier signals to form the transmission signal 38." (*Id.* at 8:17-19). Defendants' attempt to parse phrases such as "method that scrambles the phase characteristics of the modulated carrier signals in a transmission signal" to require that the signals be modulated before phase scrambling is unavailing. (D.I. 144 at 48-49). This phrase, taken from the Summary of the Invention, is nothing more than a high-level description of the transmission signal as being composed of modulated carrier signals whose phases have been scrambled. Nothing in the claims or the descriptions of

example embodiments supports Defendants' argument that the phase scrambling occurs after modulation. I will adopt Plaintiff's construction.

4. "transceiver"

a. *Plaintiff's proposed construction*: "a communications device capable of transmitting and receiving data over the same physical medium wherein the transmitting and receiving functions are implemented using at least some common circuitry"

b. *Defendants' proposed construction*: "communications device with a transmitter and receiver"

c. *Court's construction*: "communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry"

This term appears in all six of the asserted patents and the parties agree that the term should have the same construction in each claim. (D.I. 144 at 22). The parties also agree that a transceiver is a device that can both transmit and receive data. The parties dispute, however, whether the transmission and reception must occur over the same physical medium, *e.g.*, over cable or air, and whether the transmitter and receiver components of the transceiver must share common circuitry. As to the first point of dispute, there is no support in either the intrinsic or extrinsic record for the limitation that the transmission and reception of data occur over the same physical medium. Plaintiff cites only to an expert declaration to support its contention that a person of ordinary skill in the art would understand that the transmitting and receiving must occur over the same physical medium. (D.I. 144 at 25). However, nothing in the claims or specification supports this construction and Plaintiff has not pointed to any dictionary definitions or evidence other than the expert declaration to support its construction. I decline to import this limitation into the claim term.

As to the common circuitry limitation, the only information to be gleaned from the claim language itself is that the transceiver contemplated by these patents must be able to both transmit and receive data. (*See, e.g.*, '158 patent, claim 1). The specifications do not provide an explicit definition of transceiver. In the phase scrambling patents, the specification and figures indicate that the transceiver as described is a singular device housing both a transmitter portion and a receiver portion. (*Id.* at 3:31-33). These patents do not provide any specific indication that any circuitry is shared between the two. In the low power mode patents, however, the specification and figure do indicate the presence of shared components. For example, the clock, controller, and frame counter are shared by the transmitter and receiver portions of the transceiver. ('404 patent at Fig. 1).

The parties provide five different dictionary definitions for transceiver, three of which include a limitation that the transmitter and receiver share common circuitry. (D.I. 146 at A423, A433, A444, A891, A938-39). Evaluating the intrinsic evidence in light of these dictionary definitions suggests that the transmitter and receiver portions do share common circuitry or components. Therefore, I will construe transceiver to mean "a communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry."

5. "multicarrier"

   a. *Plaintiff's proposed construction*: "having multiple carrier signals that are combined as a group by simultaneous modulation to produce a transmission signal"

   b. *Defendants' proposed construction*: "having multiple carrier signals that are combined to produce a transmission signal"

   c. *Court's construction*: "having multiple carrier signals that are combined to produce a transmission signal"

The parties' only disagreement is whether this term should be construed to specify a particular method by which the carrier signals are combined. Plaintiff's opposition to Defendants' broader construction appears to stem from its disagreement with Defendants' proposed construction of "carrier." (D.I. 158 at 30:20-31:7). Since I have rejected Defendants' proposed limitations on "carrier," this concern is unwarranted. As discussed above, I have concluded that the patents disclose combination and modulation of carrier signals in the frequency domain, that is, before a time domain signal, or wave, exists. Turning to Plaintiff's proposed limitation, I find that the claim language itself does not impose any limitation on how the carrier signals are to be combined. Nor does the specification provide such limitations. Therefore, I will adopt Defendants' proposed construction.

6. "bit scrambler"

a. *Plaintiff's proposed construction*: "a component that pseudo-randomly changes the value of a bit"

b. *Defendants' proposed construction*: "component that pseudo-randomly inverts the bits in a byte of data one bit after another"

c. *Court's construction*: "component that pseudo-randomly changes the value of a bit"

The parties disagree on two points in their proposed constructions of this term: first, whether the bit scrambler operates on a byte of data; and second, whether the bits are scrambled in sequence, one after another. The parties' disagreement appears to center around whether a person of ordinary skill in the art would find that a bit scrambler is different from a byte scrambler. I do not think it is necessary to resolve this disagreement as the patent itself provides sufficient guidance as to the meaning of "bit scrambler."

The word "byte" does not appear in either the claims or specification of the '243 patent. The patent refers to "scrambling, using the bit scrambler, a plurality of input bits." ('243 patent,

claim 1). A plurality of input bits simply means more than one input bit. A byte of data is commonly understood to consist of eight bits of data. *See, e.g.*, OXFORD ENGLISH DICTIONARY (2d ed. 1989), *available at* http://www.oed.com/oed2/00030648 (defining byte as "[a] group of eight consecutive bits operated on as a unit in a computer"). There is no basis in the claim itself or in the specification for requiring that the "plurality of input bits" consist of a byte, or eight bits, of data. Nor is there any indication in the patent that the data must be presented to the scrambler a byte at a time. Rather, as Defendants themselves point out, the data is presented a bit at a time. Defendants cite the ADSL standards as extrinsic evidence of what a person of ordinary skill would understand a "bit scrambler" to be. (D.I. 144 at 52-53). The device described in the standards, however, is simply called a "scrambler," not a "bit scrambler." (D.I. 145 at A503). Furthermore, the standards show that data is input to this scrambler a byte at a time, not as a serial bit stream. (*Id.*). This is inconsistent with the bit scrambler described in the specification.

As to Defendants' argument that the scrambling must be performed sequentially, the claim language does not support such a limitation. The claim itself is indifferent to whether the scrambling is sequential, stating that the bit scrambler scrambles "a plurality of input bits to generate a plurality of output bits." (*Id.*). The specification states that the bit scrambler "receives the input serial bit stream" and, after scrambling, passes the bits to the QAM encoder. (*Id.* at 5:6-9). The QAM encoder is described as "receiving an input serial data bit stream." (*Id.* at 3:63-64). This seems to indicate that the input and output of the bit scrambler are both serial. This does not mean, however, that the scrambling itself necessarily takes place sequentially. Therefore, the intrinsic evidence does not support Defendants' proposed limitations and I will adopt Plaintiff's construction.

B. The Low Power Mode Patents

The '404 patent is directed to a multicarrier transmission system with low power sleep mode and rapid-on capability. Claim 6 is representative and reads as follows:

> 1. An *apparatus comprising a transceiver operable to*:
> receive, in a full power mode, a plurality of superframes, wherein the superframe comprises a plurality of *data* frames followed by a *synchronization frame*;
> receive, in the full power mode, a *synchronization signal*;
> transmit a message to enter into a *low power mode*;
> *store, in the low power mode, at least one parameter* associated with the full power mode operation *wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter*;
> receive, in the *low power mode*, a *synchronization signal*; and
> exit from the *low power* [sic] and restore the full power mode by using the at least one parameter and without needing to reinitialize the transceiver.

('404 patent, claim 6) (disputed terms italicized).

The '268 patent is also directed to a multicarrier transmission system with low power sleep mode and rapid-on capability. Claim 4 is representative and reads as follows:

> 4. A method, in a multicarrier transceiver, comprising:
> transmitting or receiving a message to enter a *low power mode*;
> entering the *low power mode*, wherein a transmitter portion of the transceiver does not transmit *data* during the *low power mode* and a receiver portion of the transceiver receives *data* during the *low power mode*; and
> *storing, during the low power mode, at least one parameter* associated with a full power mode.

('268 patent, claim 4) (disputed terms italicized).

1. "low power mode"

   a. *Plaintiff's proposed construction*: "a state of operation in which power is consumed, but the amount of power consumed is less than when operating in a state with full data transmission capabilities"

   b. *Defendants' proposed construction*: "state of operation in which available power is reduced"

c. *Court's construction*: "state of operation in which power is consumed, but the amount of power consumed is less than when operating in a state with full data transmission capabilities"

The primary dispute between the parties with respect to this term appears to center on whether low power mode requires that less power be supplied to the circuitry or whether less power is consumed by the device. The parties also disagree about whether the claimed "low power mode" includes both the "sleep mode" and "idle state/mode" described in the specification.

Neither sleep mode nor idle state/mode are mentioned in any of the claims. Defendants expended significant effort both in briefing and at oral argument to argue that "idle state" is not a low power mode. I disagree. The specification states in a number of different places that the invention could be incorporated into a computer and that it would be desirable in that situation that it could "enter a 'sleep' mode in which it consumes reduced power." ('404 patent at 6:2-3). The specification describes this as an "'idle' state . . . similar in many ways to the sleep mode state." (*Id.* at 6:19:24). Defendants argue that it is significant that the specification sometimes calls this a "state" instead of a "mode." (D.I. 158 at 21:10-22:3). I do not think so. Elsewhere in the specification, the same idle state is referred to as an "idle mode." ('404 patent at 8:63). It seems to me that sleep mode and idle state/mode are both low power modes implemented in different contexts.

The dispute over whether low power mode is achieved through lower power consumption or lower power supply is readily resolved by looking to the claim language. Low power mode appears in independent claims 1, 6, 11, and 16 of the '404 patent. Although claim 1 of the '404 patent is not asserted, "we look to the words of the claims themselves, both asserted and nonasserted, to define the scope of the patented invention." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). Claims 1 and 11 read, in part, "[enter/entering] into the low

power mode by reducing a power consumption of at least one portion of a transmitter." ('404 patent, claims 1 & 11). Claims 6 and 16 do not include this phrase describing how low power mode is achieved. "Unless the patent otherwise provides, a claim term cannot be given a different meaning in the various claims of the same patent." *Georgia-Pac. Corp. v. U.S. Gypsum Co.*, 195 F.3d 1322, 1331 (Fed. Cir. 1999). Read in the context of the specification, I find no reason why the term should be given different meaning in claims 6 and 16 than it has in claims 1 and 11, which indicate that low power mode is achieved through lower consumption of power.

Finally, the parties dispute whether low power mode includes, as Defendants argue, a state in which the device is completely off. (D.I. 144 at 61). Defendants' argument on this point is inconsistent with the claims and specification. While in low power mode, the transceiver must be able to either transmit or receive a synchronization signal. ('404 patent, claims 1 and 6). The argument that some power is consumed by the transceiver even in low power mode is supported by the specification. (*Id.* at 7:44-56). For these reasons, I will adopt Plaintiff's construction.

2. "stor[e/ing], in [a/the] low power mode, at least one parameter"

   a. *Plaintiff's proposed construction*: "maintaining in memory at least one parameter associated with a mode of operation with full data transmission capabilities, while in a low power mode"

   b. *Defendants' proposed construction*: "maintain[ing] in memory throughout a/the low power mode, at least one parameter"

   c. *Court's construction*: "maintain[ing] in memory, while in low power mode, at least one parameter"

The parties first dispute whether the construction should include the limitation that the parameter must be associated with full power mode. Defendants argue that this limitation already appears in the claim language and including this in the claim construction would be superfluous. (D.I. 144 at 66). Plaintiff did not reply to this argument. I agree with Defendants. The claim

language includes this limitation already when it calls for storing "at least one parameter associated with the full power mode operation." ('404 patent, claim 6). It would be redundant to include this in the court's construction of this term.

The parties also disagree about whether the parameter must be maintained throughout the duration of the low power mode. Plaintiff argues that there is no support in the claim language for requiring a particular duration for how long the parameter is stored. (D.I. 144 at 65). Defendants counter that it is a "fundamental requirement" of the invention that the parameter be stored for the entire duration of the low power mode. (*Id.*). Reading the claim as a whole, I find it is unnecessary to include this requirement in the construction of this term. The claim specifies that the device will "exit from the low power mode and restore the full power mode by using the at least one parameter." ('404 patent, claim 6). Therefore, the rest of the claim itself implies that the parameter is stored at least until the device exits from low power mode. This is captured by the court's construction of "maintain[ing] in memory, while in low power mode, at least one parameter."

3. "wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter"

a. *Plaintiff's proposed construction*: "wherein the at least one parameter includes a fine gain parameter and/or a bit allocation parameter"

b. *Defendants' proposed construction*: "wherein the at least one parameter includes both a fine gain parameter and a bit allocation parameter"

c. *Court's construction*: "wherein the at least one parameter includes a fine gain parameter and/or a bit allocation parameter"

Plaintiff argues that its construction follows the plain language of the claim and notes that the parameters listed in the claim are not categories but rather two parameters from a list of parameters that may be stored. (D.I. 144 at 90-92). Defendants argue that the phrase "at least one of" modifies both terms, requiring that both a fine gain and a bit allocation parameter must be

stored, citing Federal Circuit case law in support of their position. (*Id.* at 91). Defendants are correct that the Federal Circuit has previously construed this same phrase to require one of each of the terms in the list as a matter of grammatical construction. *SuperGuide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 886 (Fed. Cir. 2004). As a number of district courts have recognized, however, "*SuperGuide* did not erect a universal rule of construction for all uses of 'at least one of' in all patents." *Fujifilm Corp. v. Motorola Mobility LLC*, 2015 WL 1265009, at *8 (N.D. Cal. Mar. 19, 2015).

I find that this phrase is readily construed by looking at the full context of the claim itself, without having to resort to grammatical arguments. The relevant portion of the claim reads "storing, in the low power mode, *at least one parameter* associated with the full power mode operation wherein the at least one parameter comprises at least one of a fine gain parameter and a bit allocation parameter." ('404 patent, claim 11 (emphasis added)). The phrase "at least one parameter" indicates that the patent contemplates a situation where only one parameter would be stored. Defendant's construction would require a minimum of two parameters to be stored and is, therefore, inconsistent with the plain language of the claim. For this reason, I will adopt Plaintiff's construction.

4. "fine gain parameter"

   a. *Plaintiff's proposed construction*: "a parameter used to determine power level on a per subcarrier basis"

   b. *Defendants' proposed construction*: "Indefinite"

   c. *Court's construction*: "parameter used to determine power level on a per subcarrier basis"

Defendants only argument with respect to this term is that "fine" is a word of degree and, therefore, this term is necessarily indefinite. (D.I. 144 at 68). I disagree. The claim language does

not instruct that anything be measured or adjusted, as in, "make a fine adjustment to the gain," for example. Rather, the claim instructs that a specific parameter, named the "fine gain parameter," is to be stored. Although the claim language itself does not provide specific guidance as to the meaning of this term, the specification supports Plaintiff's construction, particularly when considered in the context of the extrinsic evidence Plaintiff presents to show that a person of ordinary skill in the art would understand that "fine gain" refers to the gain on a subchannel. For example, the specification discusses the requirements of initialization, and in doing so distinguishes between "setting the channel gains" and "adjusting the fine gains on the subchannels." ('404 patent at 3:12-14). This distinction is substantially supported by the ITU-T G.992.1 Standards Plaintiff referenced in its briefing and presented at oral argument as evidence of what a person of ordinary skill in the art would understand "fine gain" to mean.[2] (D.I. 144 at 70; D.I. 190 at 121:17-122:5). Therefore, I will adopt Plaintiff's construction.

5. "bit allocation parameter"

a. *Plaintiff's proposed construction*: "parameter used to determine a number of bits to be carried by a subcarrier on a per subcarrier basis"

b. *Defendants' proposed construction*: "parameter specifying the number of bits to be carried by a subchannel"

c. *Court's construction*: "parameter used to determine a number of bits to be carried by a subcarrier on a per subcarrier basis"

The parties have two disputes in construing this term. First, they disagree on whether the parameter is used to determine the number of bits or whether it specifies the number of bits. Second, they dispute whether the parameter provides the number of bits carried by a single subcarrier or whether it provides the number of bits on a per subcarrier basis, i.e. whether the Bit

[2] The relevant time period for this understanding is January 26, 1998, the priority date of both the '404 and '268 patents.

Allocation Table referenced in the specification is itself a bit allocation parameter. As to the first dispute, limiting the term to mean "specifying" would encompass how the number of bits is determined when a Bit Allocation Table is used, as described in the exemplary embodiment. The word "determine" also encompasses the use of a table to perform this task. Defendants argue that using "determine" unduly broadens the definition. I disagree. Only if I were to limit the claim to require that the only form of a bit allocation parameter be a Bit Allocation Table would Defendants' argument carry the day. The specification describes a method for constructing the Bit Allocation Table. But it is a parameter and not the Table itself that is claimed. It is not difficult to imagine other methods of determining the number of bits to be carried that do not involve a Bit Allocation Table being the parameter that is stored. Thus, I do not limit the construction to the exemplary embodiment.

The second dispute is readily resolved by turning to the specification. The patent lists some of the requisite parameters for waking from sleep mode and "Bit Allocation Tables" is included in that list. ('404 patent at 8:6-12). It seems to me that a full Bit Allocation Table is one example of the bit allocation parameter referenced in the claims. Therefore, Defendants' argument that a bit allocation parameter is nothing more than a single entry in a Bit Allocation Table must fail. Plaintiff's position that the number of bits must be specified for each subcarrier, not just a single subcarrier, is supported by the specification and comports with the purpose of the invention, i.e., allowing a transceiver to wake from sleep mode without reinitializing. Furthermore, the claim does not limit the form of the parameter to only a Bit Allocation Table. Therefore, I will adopt Plaintiff's construction.

6. "synchronization frame"

a. *Plaintiff's proposed construction*: "a frame that indicates a superframe boundary"

b. *Defendants' proposed construction*: "frame that carries no user or overhead bit-level data and is inserted to establish superframe boundaries"

c. *Court's construction*: "frame that indicates a superframe boundary"

The parties agree that synchronization frames indicate or establish superframe boundaries. The parties disagree, however, as to whether the synchronization frame must be limited to that defined in the ITU Document G922.2. Defendants insist that it must be so limited, pointing to the specification, which references this ITU Document. ('404 patent at 5:5-12). There are two problems with Defendants' argument, however. First, the reference to the ITU document is made after the reference to data frames and is also given specifically as an example ("data frames (*e.g.*, sixty-eight frames for ADSL as specified in ITU Document G.992.2)"). No reference is made to the ITU document after the synchronization frame is mentioned. Second, this is a simply an exemplary embodiment and I find no evidence to support limiting the claim to one exemplary embodiment. Therefore, I will adopt Plaintiff's construction.

7. "synchronization signal"

a. *Plaintiff's proposed construction*: "an indication used to establish or maintain a timing relationship between transceivers"

b. *Defendants' proposed construction*: "reference wave used to establish or maintain a timing relationship between transceivers"

c. *Court's construction*: "signal used to establish or maintain a timing relationship between transceivers"

The only dispute between the parties with respect to this term is whether the signal is "an indication" or a "reference wave." Defendant argues strenuously that the signal must be a wave, arguing that all of the examples of synchronization signals given in the specification are "reference waves." (D.I. 144 at 81). Defendant does not explain, however, what exactly a reference wave is in this context. The phrase "reference wave" does not appear anywhere in the patent and

Defendant has offered no definition. I will not construe this claim term to include a phrase that adds ambiguity and uncertainty to the meaning of the term. Plaintiff's proposal of "indication," however, is little better as the word "indication" could easily be deemed to include things that are not "signals." It seems to me that "signal" is a well-understood term that has a plain meaning to those skilled in the art. I see no need to substitute a different word that would introduce ambiguity into the meaning of the term. Therefore, I will adopt Plaintiff's proposed construction, modified as follows: "signal used to establish or maintain a timing relationship between transceivers."

8. "apparatus comprising a transceiver operable to"

   a. *Plaintiff's proposed construction*: "See above for the construction of 'transceiver'; otherwise plain meaning"

   b. *Defendants' proposed construction*: "The preamble is limiting[3] and this is a means-plus-function limitation. The "transceiver" is the CPE transceiver depicted in Figure 2"

   c. *Court's construction*: "plain meaning with 'transceiver' as previously construed"

Defendants argue that this element from the preamble of several claims is limiting as a means-plus-function claim element governed by 35 U.S.C. § 112 ¶ 6 because the word transceiver does not impart definite structure. (D.I. 144 at 85). Plaintiff responds that transceiver has a well-understood structural meaning in the art. (*Id.* at 86). When the word "means" does not appear in the claim element, there is a presumption that the element is not means-plus-function. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015). "[T]he presumption can be overcome and § 112, para. 6 will apply if the challenger demonstrates that the claim term fails to 'recite sufficiently definite structure' or else recites 'function without reciting sufficient structure for performing that function.'" *Id.*

[3] Defendants argue only that the preamble provides a functional limitation. Therefore, I decline to address whether the preamble is otherwise limiting.

I conclude that § 112 ¶ 6 does not apply to this claim element. The word "means" does not appear in the claim element, so I begin with the presumption that § 112 ¶ 6 does not apply. Defendants have not overcome this presumption. Although "apparatus" is a non-structural term, the word "transceiver" imparts sufficient structure to the claim element. Transceiver is not a generic term like module or device. *Id.* at 1350. Rather, transceiver is the name of a device well known in the field of communications and, furthermore, the claimed transceiver is sufficiently described in the specification. (*See* '404 patent at 4:14-5:36). I will adopt Plaintiff's construction.

9. "data"

a. *Plaintiff's proposed construction*: "non-control information"

b. *Defendants' proposed construction*: "digital information"

c. *Court's construction*: "content"

Plaintiff initially argued that this term should be construed to have its plain meaning. (D.I. 144 at 87-88). Plaintiff proposed "non-control information" in response to Defendants' initial proposed construction, "information." (*Id.* at 89). At oral argument, Defendants proposed to narrow their construction to "digital information." (D.I. 190 at 144:21). I am not persuaded that any of these constructions provide any clarity as to the meaning of the term "data." At oral argument, I proposed construing the term to mean "content." (*Id.* at 151:21). Plaintiff agreed to this proposed construction. (*Id.* at 155:9-156:1).

Defendants, however, argue that construing data to mean "content" would impermissibly narrow the meaning of "data" in some of the claims because "user data" is used in other claims. (*Id.* at 156:4-12). According to Defendants, user data is content. This position is contradicted by the patent specification, however. The specification provides that during sleep mode, "user data provided by the CO transceiver will be benign idle data such as ATM IdleCells or HDLC Flag

octets." ('268 patent at 7:34-36). Although this information is defined to be user data by the patent itself, it is not content. Therefore, I will construe data to mean content.

C. The Diagnostic Mode Patents

The '430 patent is directed to multicarrier modulation messaging for frequency domain received idle channel noise information. Claim 1 is representative and reads as follows:

> 1. A transceiver capable of *transmitting test information over a communication channel* using multicarrier modulation comprising:
>
> a transmitter portion capable of transmitting a message, wherein the message comprises one or more data variables that represent the *test information*, wherein bits in the message are modulated onto DMT symbols using Quadrature Amplitude Modulation (QAM) with more than 1 bit per subchannel and wherein at least one data variable of the one or more data variables comprises an *array representing frequency domain received idle channel noise information.*

('430 patent, claim 1) (disputed terms italicized).

The '412 patent is directed to multicarrier modulation messaging for power level per subchannel information. Claim 1 is representative and reads as follows:

> 1. A transceiver capable of *transmitting test information over a communication channel* using multicarrier modulation comprising:
>
> a transmitter portion capable of transmitting a message, wherein the message comprises one or more data variables that represent the *test information*, wherein bits in the message are modulated onto DMT symbols using Quadrature Amplitude Modulation (QAM) with more than 1 bit per subchannel and wherein at least one data variable of the one or more data variables comprises an *array representing power level per subchannel information.*

('412 patent, claim 1) (disputed terms italicized).

1. "[transmitting/receiving] test information over a communication channel"

   a. *Plaintiff's proposed construction*: "plain meaning"

   b. *Defendants' proposed construction*: "transmitting/receiving test information to/from a central office modem"

   c. *Court's construction*: "plain meaning"

Defendants seek to import a limitation into this claim requiring that the test information be transmitted either to or from a central office modem. This limitation is unsupported by either the claims or the specification. The specification does indicate that the receiving transceiver is "typically located" at the central office, but typically does not mean always. ('412 patent at 1:53). Defendants argue that the patent is directed to the solution of a particular problem: diagnosing problems without the need to dispatch a technician to the customer's home. (D.I. 144 at 97). This may be a problem identified in the specification that is solved by this patent, but the solution to the problem is not so limited. I find no basis for importing this limitation into the claim. I agree with Plaintiff that this term should be given its plain meaning. Defendants are prohibited from arguing that the term is limited to communications over a channel that includes the central office modem.

2. "test information"

   a. *Plaintiff's proposed construction*: "information relating to a measured characteristic of a communication channel"

   b. *Defendants' proposed construction*: "information relating to a disturbance in the communication channel"

   c. *Court's construction*: "information relating to a characteristic of a communication channel or the communications equipment operating on that channel"

The parties dispute whether the test information must be measured and whether the information must relate to a disturbance in the communications channel. I find that neither of these limitations is supported by the intrinsic evidence.

Defendants contend that the description of the invention as a whole in the specification is limiting and that test information must therefore be limited to information "relate[d] to the diagnosis and resolution of communications problems caused by a disturbance on a communications channel." (D.I. 144 at 102). Defendants' argument is unavailing. The

specification states, "The systems and methods of this invention are directed toward reliably exchanging diagnostic and test information between transceivers over a digital subscriber line in the presence of voice communications and/or other disturbances." ('430 patent at 1:44-47). Nothing in this description provides any limitation on the definition of test information. The reference to disturbances means only that the invention provides a method for the exchange of test information when there is a disturbance on the line. The specification later provides an extensive, but not exhaustive, list of what test information might include. (*Id.* at 2:24-43). Many of the items in this list are unrelated to disturbances. It would be inappropriate to limit the definition of test information when nothing in the specification indicates such a limitation.

With respect to whether the information must be measured, Plaintiff argues that a person of ordinary skill in the art would recognize that the test information as claimed must be measured. (D.I. 144 at 105). Defendants counter that the specification includes a list of categories of information that may be included as the test information and that a number of the items on the list, such as Chip Type, do not require measurement to determine. (*Id.* at 104). I agree with Defendants. Although some types of test information, as defined in the specification, must be measured, other types are simply characteristics of the communications system.

Defendants further challenge Plaintiff's construction as improperly limiting the test information to characteristics of a communications channel. (*Id.*) Defendants point out that information such as Chip Type and Vendor ID are characteristics of the modems, not of the communications channel itself. (*Id.*). I agree with Defendants. The test information defined in the specification appears to more broadly encompass information related not only to the communications channel itself, but also to the equipment used at one end of the channel. Therefore, I will adopt the following construction for test information: "information relating to a

characteristic of a communication channel or the communications equipment operating on that channel."

3. "array representing frequency domain received idle channel noise information"

   a. *Plaintiff's proposed construction*: "ordered set of values representative of noise in the frequency domain measured on respective subchannels while no input signals are being transmitted on the subchannels"

   b. *Defendants' proposed construction*: "ordered set of values representative of noise in the frequency domain that was received by a transceiver on a channel in the absence of a transmission signal"

   c. *Court's construction*: "ordered set of values representative of noise in the frequency domain that was received by a transceiver on respective subchannels in the absence of a transmission signal"

The parties have three disputes with respect to this term: whether the values must be measured; whether the values represent noise on a subchannel basis; and whether the idle channel noise corresponds to "no input signals" being transmitted or simply "the absence of a transmission signal." The first and third disputes are readily resolved. There is no indication, either in the claims or in the specification, as to how these values are obtained. Certainly the values may be measured, but I cannot find support in the intrinsic evidence to limit the construction to measured values only. Furthermore, Plaintiff's own extrinsic evidence, and the only evidence presented with respect to the meaning of "idle channel noise," indicates that Defendants propose the better construction. *See* NEWTON'S TELECOM DICTIONARY 410 (15th ed. 1999) (defining idle channel noise as "[n]oise which exists in a communications channel when no signals are present"). There is no support for limiting idle channel noise to noise present in the absence of "input signals." Therefore, as to these two disputes, I adopt Defendants' proposed construction.

As to the dispute over whether the values are measured on respective subchannels, I find Defendants' arguments unavailing. Defendants are correct to point out that the applicants used the

phrase "per subchannel" explicitly in the '412 patent. ('412 patent, claim 1). However, the "array" terms of the two patents are differently worded. Thus, the absence of this phrase in the claims of the '430 patent does not necessarily render the phrase superfluous in the '412 patent. Furthermore, the fact that what is claimed is an "array" implies that more than one value is included. Therefore, I decline to adopt either party's proposed construction and instead will construe this term to mean "ordered set of values representative of noise in the frequency domain that was received by a transceiver on respective subchannels in the absence of a transmission signal."

4. "array representing power level per subchannel information"

   a. *Plaintiff's proposed construction*: "ordered set of values representative of power levels measured on respective subchannels"

   b. *Defendants' proposed construction*: "ordered set of values representative of power levels of respective subchannels"

   c. *Court's construction*: "ordered set of values representative of power levels of respective subchannels"

The parties' only dispute with respect to this term is whether the values must be measured. Plaintiff argues that without specifying that the values are measured, the term could be understood to mean that the values represent power level settings. (D.I. 144 at 115). Plaintiff further argues that the very definition of test information requires that the values be measured. (*Id.* at 116). I have already rejected the argument that all test information must be measured, however. Plaintiff cites to dependent claims specifying that the power levels are "based on a Reverb signal" and, therefore, must be measured. (*Id.*). Plaintiff further points to the specification, which provides that the power levels are "detected during the ADSL Reverb signal." (*Id.*). Defendants counter that detecting is not the same as measuring and that nothing in the claims or specification require that "the *only* way to obtain power level information is to measure it." (*Id.* at 117). Defendants

further argue that there is a presumption that a limitation present in a dependent claim is not present in the independent claim. (*Id.*).

As an initial matter, I reject Defendants' argument that detect and measure have different meanings in this context. I do, however, agree with Defendants argument that the limitation in the dependent claim should not be imported into the independent claim. Plaintiff's citations to the specification describe a preferred embodiment which, it seems to me, directly corresponds with the dependent claims. While I do not see any reason these power levels could not be measured, or that they must be obtained in any particular way, I also do not see any support for requiring that they be measured. Therefore, I will adopt Defendants' proposed construction.

5. "Reverb signal"

   a. *Plaintiff's proposed construction*: "a signal generated by modulating carriers in a multicarrier system with a known pseudo-random sequence to generate a wideband modulated signal"

   b. *Defendants' proposed construction*: "any 'REVERB' signal defined in the ITU or ANSI ADSL standards in existence as of January 8, 2001"

   c. *Court's construction*: "signal generated by modulating carriers in a multicarrier system with a known pseudo-random sequence to generate a wideband modulated signal"

The primary dispute between the parties with respect to this construction is whether, as Defendants argue, the Reverb signal is limited to that defined in the referenced standards. Defendants find support for this limitation both in the fact that the term is capitalized, which Defendants take to indicate a reference to the REVERB1 signal from the standards, as well as from the reference to the standards in the specification. (D.I. 144 at 112-13). I find Defendants' argument unconvincing. Although the term "Reverb" is capitalized in the claims, it is not spelled out in all capital letters, nor does it include the number "1" at the end. Everywhere the specific standard is mentioned in the specification, it is given as "REVERB1." ('412 patent at 3:57-4:3).

If the applicant had meant to claim the specific REVERB1 signal from the relevant standards, it seems likely he would have named that specific signal in the claim. The specification refers to the REVERB1 signal from the standards when describing an exemplary embodiment and there is no evidence in the specification of any disclaimer of other ways of generating a Reverb signal.

Plaintiff's proposed construction, on the other hand, is drawn directly from the specification. (*Id.* at 3:62-64). The applicant chose to define how the Reverb signal was to be generated. Having found no compelling reason to impose additional limitations on the meaning of this term, I will adopt Plaintiff's construction.

IV. CONCLUSION

Within five days the parties shall submit a proposed order consistent with this Memorandum Opinion suitable for submission to the jury.

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bioelectric null (zero lead) (medical electronics). A region of tissue or other area in the system, which has such electric symmetry that its potential referred to infinity does not significantly change. *Note:* This may or may not be ground potential. 192

bionics (computer applications). A branch of technology relating the functions, characteristics, and phenomena of living systems to the development of mechanical systems. 571

Biot-Savart law. *See:* **magnetic field strength produced by an electric current.**

biparting door (elevator). A vertically sliding or a horizontally-sliding door, consisting of two or more sections so arranged that the sections or groups of sections open away from each other and so interconnected that all sections operate simultaneously. *See:* **hoistway (elevator or dumbwaiter).** 328

bipolar (power supplies). Having two poles, polarities, or directions. *Note:* Applied to amplifiers or power supplies, it means that the output may vary in either polarity from zero: as a symmetrical program it need not contain a direct-current component. *See:* **unipolar.** 228

bipolar device (circuits and systems). An electronic device whose operation depends on the transport of both holes and electrons. 67

bipolar electrode. An electrode, without metallic connection with the current supply, one face of which acts as an anode surface and the opposite face as a cathode surface when an electric current is passed through the cell. *See:* **electrolytic cell.** 328

bipolar electrode system (electrobiology). Either a pickup or stimulating system consisting of two electrodes whose relation to the tissue currents is roughly symmetrical. *See:* **electrobiology.** 192

bipolar pulse (pulse terms). Two pulse waveforms of opposite polarity which are adjacent in time and which are considered or treated as a single feature. 254

bipolar video (radar). A radar video signal whose amplitude can have both positive and negative values; derived from a synchronous phase detection process. Coherent detection produces one type of bipolar video. 13

biquinary. Pertaining to the number representation system in which each decimal digit *N* is represented by the digit pair *AB,* where N = 5A + B, and where A = 0 or 1 and B = 0,1,2,3, or 4; for example, decimal 7 is represented by biquinary 12. This system is sometimes called a mixed-radix system having the radices 2 and 5. 255

birefringence. *See:* **birefringent medium.**

birefringent medium (fiber optics). A material that exhibits different indices of refraction for orthogonal linear polarizations of the light. The phase velocity of a wave in a birefringent medium thus depends on the polarization of the wave. Fibers may exhibit birefringence. *See:* **refractive index (of a medium).** 433

bistable (1) (general). The ability of a device to assume either of two stable states. 206

(2) (industrial control). Pertaining to a device capable of assuming either one or two stable states. *See:* **control system, feedback.** 255

bistable amplifier (industrial control). An amplifier with an output that can exist in either of two stable states without a sustained input signal and can be switched abruptly from one state to the other by specified inputs. *See:* **control system, feedback; rating and testing magnetic amplifiers.** 206

bistable logic function (graphic symbols for logic functions). A sequential logic function that has two and only two internal output states. *Syn:* **flip-flop.** 88, 451

bistable operation. Operation of a charge-storage tube in such a way that each storage element is inherently held at either of two discrete equilibrium potentials. *Note:* Ordinarily this is accomplished by electron bombardment. *See:* **charge-storage tube.** 174

bistatic cross section (antennas). The scattering cross section in any specified direction other than back toward the source. *See:* **monostatic cross section; radar cross section** 111

bistatic radar. A radar using antennas at different locations for transmission and reception. 13

bit (1)(microprocessor operating systems). A contraction of the term 'binary digit'; a unit of information represented by either a zero or a one. 434, 478

(2)(supervisory control, data acquisition, and automatic control). (A) Least significant. In an n bit binary word its contribution is (0 or 1) toward the maximum word value of (2n-1). (B) Most significant. In an n bit binary word its contribution is (0 or 1 times 2(n-1) toward the maximum word value of (2n-1). 570

(3) (data transmission). (A) An abbreviation of 'binary digit'. (B) A single occurrence of a character in a language employing exactly two kinds of characters. (C) A unit of storage capacity. The capacity, in bits, of a storage device with logarithm to the base two of the number of possible states of the device. 59

(4) (information theory). A unit of information content equal to the information content of a message the *a priori* probability of which is one-half. *Note:* If, in the definition of information content, the logarithm is taken to the base two, the result will be expressed in bits. One bit equals $\log_{10} 2$ hartley. *See:* **information theory; check bit; parity bit.** 61

(5) (electronic computers). (A) An abbreviation of binary digit. (B) A single occurrence of a character in a language employing exactly two distinct kinds of characters. (C) A unit of storage capacity. The capacity, in bits, of a storage device is the logarithm to the base two of the number of possible states of the device. *See:* **storage capacity.** 54, 235

bit error. *See:* **error rate.**

bit-parallel (programmable instrumentation)(signals and paths)(696 interface devices). A set of concurrent data bits present on a like number of signal lines used to carry information. Bit-parallel data bits may be acted upon concurrently as a group or independently as individual data bits. 40, 378,538

bit rate (1)(supervisory control, data acquisition, and automatic control)(station control and data acquisition). The number of bits transferred in a given time interval. Bits per second is a measure of the rate at which bits are transmitted. 403, 570

EXHIBIT H

PTO/SB/0:
Approved for use through 07/31/2006 OMB 0
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	T3653-9285US01
First Named Inventor	TZANNES, MARCOS C.
Title	SHARING MEMORY AND PROCESSING RESOURCES IN DSL SYSTEMS
Express Mail Label No.	

ADDRESS TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPLICATION ELEMENTS

See *MPEP chapter 600 concerning utility patent application contents.*

1. ☒ **Fee Transmittal Form** (e.g., PTO/SB/17)
   (Submit an original and a duplicate for fee processing)
2. ☐ **Applicant claims small entity status**
   See 37 CFR 1.27
3. ☒ **Specification** *[Total Pages 30]*
   Both the claims and abstract must start on a new page
   (For information on the preferred arrangement, see MPEP 608.01(a))
4. ☒ **Drawing(s)** *(35 U.S.C. 113)* *[Total Sheets 3]*
5. **Oath or Declaration** *[Total Sheets _____]*
   a. ☐ Newly executed (original or copy)
   b. ☐ Unexecuted (original or copy)
   c. ☐ A copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 18 completed)
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
6. ☒ **Application Data Sheet.** See 37 CFR 1.76
7. ☐ **CD-ROM or CD-R** in duplicate, large table or Computer Program (Appendix)
   ☐ Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission**
   (if applicable, items a.-c. are required
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
   i ☐ CD-ROM or CD-R (2 copies; or
   ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☐ **Assignment Papers** (cover sheet & document(s))
   Name of Assignee _____
10. ☐ **37 CFR 3.73(b) Statement** ☐ **Power of Attorney**
    (when there is an assignee)
11. ☐ **English Translation Document** *(if applicable)*
12. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    ☐ Copies of citations enclosed
13. ☐ **Preliminary Amendment**
14. ☒ **Return Receipt Postcard** (MPEP 503)
    (Should be specifically itemized)
15. ☐ **Certified Copy of Priority Document(s)**
    (if foreign priority is claimed)
16. ☐ **Nonpublication Request** under 35 U.S.C. 122(b)(2)(B)(i).
    Applicant must attach form PTO/SB/35 or equivalent
17. ☐ Other: _____

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 60/618,269

Prior application information: Examiner _____ Art Unit: _____

19. CORRESPONDENCE ADDRESS

☒ The address associated with Customer Number: 000181 or ☐ *Correspondence address below*

Name					
City		State		Zip Code	
Country		Telephone		Fax	

Signature	Jason H. Vick	Date	October 11, 2005
Name (Print/Type)		Registration No. (Attorney/Agent)	45,285

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO t an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of C P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. 1450, Alexandria, VA 22313-1450.**

13281
101105
U.S. PTO

PTO/SB/17 (12-04v2)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Effective on 12/8/2004
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818)

FEE TRANSMITTAL For FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	$2,650.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	TZANNES, MARCOS C.
Examiner Name	
Art Unit	
Attorney Docket No.	T3653-9285US01

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify):_____

☒ Deposit Account Deposit Account Number: 50-1165 Deposit Account Name: Miles & Stockbridge P.C.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) ☒ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	**Fee ($)**	**Fee ($)**	**Fee ($)**	**Fee ($)**	**Fee ($)**	**Fee ($)**	**Fees Paid ($)**
Utility	300	150	500	250	200	100	**$1,000.00**
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	**Fee ($)**	**Small Entity Fee ($)**
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	**Extra Claims**	**Fee ($)**	**Fee Paid ($)**
45 - 20 or HP =	25	x 50.00	= **$1250.00**

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	**Extra Claims**	**Fee ($)**	**Fee Paid ($)**
5 - 3 or HP =	2	x 200.00	= **$400.00**

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	**Extra Sheets**	**Number of each additional 50 or fraction thereof**	**Fee ($)**	**Fee Paid ($)**
_____ - 100 =	_____ / 50 =	_____ (round up to a whole number) x	_____ =	_____

4. OTHER FEE(S)

Fee Paid ($)

Non-English Specification, $130 fee (no small entity discount) _____

Other (e.g., late filing surcharge): _____ _____

SUBMITTED BY				Complete *(if applicable)*	
Signature		Registration No. *(Attorney/Agent)*	45,285	Telephone	(703) 903-9000
Name *(Print/Type)*	Jason H. Vick			Date	October 11, 2005

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.
DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Claims:

1. A method for sharing resources in a transceiver comprising:

allocating a first portion of shared memory to a first latency path and allocating a second portion of the shared memory to a second latency path.

2. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

3. The method of claim 1, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

4. The method of claim 1, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

5. The method of claim 1, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

6. The method of claim 1, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

7. The method of claim 1, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

8. The method of claim 1, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

9. The method of claim 8, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

10. A transceiver comprising:

a first portion of shared memory that is allocated to a first latency path; and

a second portion of the shared memory that is allocated to a second latency path.

11. The transceiver of claim 10, further comprising:

an allocation module designed to allocate the shared memory based on one or more communication parameters.

12. The transceiver of claim 11, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate (BER).

13. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

14. The transceiver of claim 10, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

15. The transceiver of claim 10, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

16. The transceiver of claim 10, further comprising a shared resource management module designed to determine information that is transmitted to another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

17. The transceiver of claim 10, further comprising a shared resource management module designed to utilize information that is received from another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated.

18. The transceiver of claim 10, further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules.

19. A system for sharing resources in a transceiver comprising:

means for allocating a first portion of shared memory to a first latency path and means for allocating a second portion of the shared memory to a second latency path.

20. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

21. The system of claim 19, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

22. The system of claim 19, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

23. The system of claim 19, further comprising means for transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

24. The system of claim 19, further comprising means for receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

25. The system of claim 19, further comprising means for allocating a shared processing module to a plurality of coding and/or decoding modules.

26. The system of claim 19, wherein the allocating of at least one portion

of the shared memory is based on one or more communication parameters.

27. The system of claim 26, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

28. A protocol for sharing resources in a transceiver comprising:

allocating a first portion of shared memory to a first latency path and allocating a second portion of the shared memory to a second latency path.

29. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

30. The protocol of claim 28, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

31. The protocol of claim 28, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

32. The protocol of claim 28, further comprising transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

33. The protocol of claim 28, further comprising receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

34. The protocol of claim 28, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

35. The protocol of claim 28, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

36. The protocol of claim 35, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

37. An information storage media having stored thereon information that when executed allows sharing of resources in a transceiver comprising:

information that allocates a first portion of shared memory to a first latency path and information that allocates a second portion of the shared memory to a second latency path.

38. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.

39. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver.

40. The media of claim 37, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver.

41. The media of claim 37, further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

42. The media of claim 37, further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

43. The media of claim 37, further comprising information that allocates a shared processing module to a plurality of coding and/or decoding modules.

44. The media of claim 37, wherein the allocating of at least one portion of

the shared memory is based on one or more communication parameters.

45. The media of claim 44, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

UNITED STATES PATENT AND TRADEMARK OFFICE

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/246,163	10/11/2005	Marcos C. Tzannes	5550-54	5478

62574 7590 12/09/2009

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

EXAMINER	
PFIZENMAYER, MARK C	
ART UNIT	PAPER NUMBER
2447	

NOTIFICATION DATE	DELIVERY MODE
12/09/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jvick@sheridanross.com

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No.	Applicant(s)	
	11/246,163	TZANNES ET AL.	
	Examiner	Art Unit	
	MARK PFIZENMAYER	2447	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/22/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 19 and 28 were amended in the amendment filed on 8/21/2009. The claims 1-45 are pending.

Response to Arguments

2. Applicant's arguments filed 8/21/2009 have been fully considered but they are not persuasive.

A. Applicant argues the cited prior art does not teach how the same memory can be used for simultaneously receiving of data and transmitting data.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the same memory being used for simultaneously receiving of data and transmitting data) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Specification

3. The disclosure is objected to because of the following informalities:

- The specification fails to provide proper antecedent basis for "an information storage media" in claim 37. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Appropriate correction is required.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 19-36 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

With respect to claim 19, the claim lacks the necessary physical articles or objects to constitute a machine or a manufacture within the meaning of 35 U.S.C. 101. They are clearly not a series of steps or acts to be a process nor are they a combination of chemical compounds to be a composition of matter. As such, they fail to fall within a statutory category. They are, at best, functional descriptive material per se. Claims 20-27 are likewise rejected.

With respect to claim 28, the claim lacks the necessary physical articles or objects to constitute a machine or a manufacture within the meaning of 35 U.S.C. 101. They are clearly not a series of steps or acts to be a process nor are they a combination of chemical compounds to be a composition of matter. As such, they fail to fall within a statutory category. They are, at best, functional descriptive material per se. MPEP §2106.01. Claims 29- 36 are likewise rejected.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Fadavi-Ardekani (U.S. Patent No. 6,707,822).

With respect to claim 1, Fadavi-Ardekani teaches a method for sharing resources in a transceiver (i.e., the IDIM of the transceiver can support different number of sessions; lines 3-5 in column 7) comprising: allocating a first portion of shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and allocating a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 2, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 3, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 4, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e.,

the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 5, Fadavi-Ardekani further teaches transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 6, Fadavi-Ardekani further teaches receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 7, Fadavi-Ardekani further teaches allocating a shared processing module to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking,

scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 8, Fadavi-Ardekani further teaches wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 9, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (i.e., interleave depth, wherein the interleave depth is directly proportional to latency, lines 3-5 in column 7).

With respect to claim 10, Fadavi-Ardekani teaches a transceiver comprising: a first portion of shared memory that is allocated to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7); and a second portion of the shared memory that is allocated to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 11, Fadavi-Ardekani further teaches further comprising: an allocation module designed to allocate the shared memory based on one or more communication parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 12, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate

(i.e., interleave depth, wherein the interleave depth is directly proportional to latency, lines 3-5 in column 7).

With respect to claim 13, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 14, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 15, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 16, Fadavi-Ardekani further teaches further comprising a shared resource management module designed to determine information that is transmitted to another transceiver, wherein the information is used to determine a

maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 17, Fadavi-Ardekani further teaches further comprising a shared resource management module designed to utilize information that is received from another transceiver, wherein the information is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 18, Fadavi-Ardekani further teaches further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking, scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 19, Fadavi-Ardekani teaches a system for sharing resources in a transceiver (i.e., the IDIM of the transceiver can support different number of sessions; lines 3-5 in column 7) comprising: means for allocating a first portion of

shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and means for allocating a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 20, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 21, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 22, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 23, Fadavi-Ardekani further teaches means for transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 24, Fadavi-Ardekani further teaches means for receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 25, Fadavi-Ardekani further teaches means for allocating a shared processing module to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking, scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 26, Fadavi-Ardekani further teaches wherein the allocating of at least one portion of the shared memory is based on one or more communication

parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 27, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (i.e., interleave depth, wherein the interleave depth is directly proportional to latency, lines 3-5 in column 7).

With respect to claim 28, Fadavi-Ardekani teaches a protocol for sharing resources in a transceiver (i.e., the IDIM of the transceiver can support different number of sessions; lines 3-5 in column 7) comprising: allocating a first portion of shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and allocating a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 29, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 30, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to

allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 31, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 32, Fadavi-Ardekani further teaches transmitting to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 33, Fadavi-Ardekani further teaches receiving from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 34, Fadavi-Ardekani further teaches allocating a shared processing module to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking, scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 35, Fadavi-Ardekani further teaches wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 36, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (i.e., interleave depth, wherein the interleave depth is directly proportional to latency, lines 3-5 in column 7).

With respect to claim 37, Fadavi-Ardekani teaches sharing of resources in a transceiver (i.e., the IDIM of the transceiver can support different number of sessions; lines 3-5 in column 7) comprising: information that allocates a first portion of shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and information that allocates a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7).

With respect to claim 38, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes an interleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new interleave session may be added to an existing interleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 39, Fadavi-Ardekani further teaches wherein the first latency path includes an interleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave; lines 3-5 and 30-33 in column 7).

With respect to claim 40, Fadavi-Ardekani further teaches wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver (i.e., the size of the IDIM and the interleave depth may be modified to allocate multiple portions, wherein each portion or session may be used for interleave or deinterleave. For example, a new deinterleave session may be added to an existing deinterleave session; lines 3-5 and 30-33 in column 7).

With respect to claim 41, Fadavi-Ardekani further teaches further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein

overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 42, Fadavi-Ardekani further teaches further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated (i.e., the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes, wherein overhead data bytes may contain information that is used to determine a maximum amount of shared memory that can be allocated, lines 20-25 in column 2).

With respect to claim 43, Fadavi-Ardekani further teaches further comprising information that allocates a shared processing module to a plurality of coding and/or decoding modules (i.e., the FCI supports multiple ADSL sessions and performs various tasks on payload data including framing/de-framing, cyclic redundancy check generation/checking, scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving, lines 11-17 in column 6).

With respect to claim 44, Fadavi-Ardekani further teaches wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters (i.e., the number of sessions supported is based on the size of the IDIM and the interleave depth, lines 3-5 and 30-33 in column 7).

With respect to claim 45, Fadavi-Ardekani further teaches wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (i.e., interleave depth, wherein the interleave depth is directly proportional to latency,

lines 3-5 in column 7).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARK PFIZENMAYER whose telephone number is (571)270-7214. The examiner can normally be reached on Monday - Friday 8:00 - 5:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Hwang can be reached on (571)272-4036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mark Pfizenmayer
Patent Examiner
1 December 2009

/Joon H. Hwang/
Supervisory Patent Examiner, Art Unit 2447

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/246,163	10/11/2005	Marcos C. Tzannes	5550-54	5478

62574 7590 12/16/2009

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

EXAMINER	
PFIZENMAYER, MARK C	
ART UNIT	PAPER NUMBER
2447	

NOTIFICATION DATE	DELIVERY MODE
12/16/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jvick@sheridanross.com

PTOL-90A (Rev. 04/07)

Interview Summary	**Application No.** 11/246,163	**Applicant(s)** TZANNES ET AL.	
	Examiner BENJAMIN R. BRUCKART	**Art Unit** 2446	

All participants (applicant, applicant's representative, PTO personnel):

(1) *BENJAMIN R. BRUCKART*.

(2) *Pfizenmayer, Mark*.

(3)*Jason H Vick, Reg. No. 45, 285*.

(4)*Inventor Marcos Tzannes*.

Date of Interview: *08 December 2009*.

Type: a)☐ Telephonic b)☐ Video Conference
c)☒ Personal [copy given to: 1)☒ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☐ No.
If Yes, brief description: _____.

Claim(s) discussed: *1*.

Identification of prior art discussed: *N/A*.

Agreement with respect to the claims f)☐ was reached. g)☒ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *See Continuation Sheet*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

/Benjamin R Bruckart/ Primary Examiner, Art Unit 2446	

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Continuation of Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: The examiner and applicant discussed an overview of the invention and explained features of simultaneous transfer and types of interleaving and allocation of memory based on direction of transmission and bandwidth. The examiner felt the proposed amendment was a step in the right direction but that more details would be recommended to overcome the cited prior art. The examiner suggested the features of need more detailing such as type of memory, type of interleaving to distinguish from the prior art or memory art. .

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of: Tzannes et al.	Group Art Unit: 2447
Application No.: 11/246,163	Examiner: Pfizenmayer, M.
Filed: October 11, 2005	Confirmation No.: 5478
Atty. File No.: 5550-54	

For: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

SUPPLEMENTAL AMENDMENT AND RESPONSE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit this Amendment and Response supplemental to the Amendment and Response and RCE filed December 17, 2009. Please credit any overpayment or charge any underpayment to Deposit Account No. 19-1970.

Please amend the above-identified patent application as follows:

Amendments to the Claims are shown in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 5 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 45. (Cancelled)

46. (Currently Amended) A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization indicating a maximum number of bytes of memory that can be allocated to an interleaver;

allocating, in the transceiver, a first number of bytes of a shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate; and

allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate,

wherein the allocated memory for the interleaver does not exceed the maximum number of bytes indicated in the message, and

wherein the shared memory is used to simultaneously interleave the first plurality of RS coded data bytes and deinterleave the second plurality of RS coded data bytes.

47. (Previously Presented) The method of claim 46, wherein the allocating is based on an impulse noise protection requirement.

48. (Previously Presented) The method of claim 46, wherein the allocating is based on a latency requirement.

49. (Previously Presented) The method of claim 46, wherein the allocating is based on a bit error rate requirement.

50. (Currently Amended) A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization indicating a maximum number of bytes of memory that can be allocated to a deinterleaver;

allocating, in the transceiver, a first number of bytes of a shared memory to an interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate; and

allocating, in the transceiver, a second number of bytes of the shared memory to the deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate,

wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes indicated in the message, and

wherein the shared memory is used to simultaneously interleave the first plurality of RS coded data bytes and deinterleave the second plurality of RS coded data bytes.

51. (Previously Presented) The method of claim 50, wherein the allocating is based on an impulse noise protection requirement.

52. (Previously Presented) The method of claim 50, wherein the allocating is based on a latency requirement.

53. (Previously Presented) The method of claim 50, wherein the allocating is based on a bit error rate requirement.

REMARKS

Applicants respectfully request reconsideration of this application as amended.

By this amendment, claims 46 and 50 have been amended to correct a typographical error. The combination of features in all the above claims is neither taught nor suggested by the cited reference.

A Notice of Allowance is earnestly solicited.

The Commissioner is hereby authorized to charge to deposit account number 19-1970 any fees under 37 CFR § 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby petitioned.

Respectfully submitted,

SHERIDAN ROSS P.C.

Date: 8 Mar '10

By: _____

Jason H. Vick
Reg. No. 45,285
1560 Broadway, Suite 1200
Denver, Colorado 80202
Telephone: 303-863-9700

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NOTICE OF ALLOWANCE AND FEE(S) DUE

62574 7590 09/07/2010

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

EXAMINER	
PFIZENMAYER, MARK C	
ART UNIT	PAPER NUMBER
2447	

DATE MAILED: 09/07/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/246,163	10/11/2005	Marcos C. Tzannes	5550-54	5478

TITLE OF INVENTION: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/07/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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62574 7590 09/07/2010

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

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(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/246,163	10/11/2005	Marcos C. Tzannes	5550-54	5478

TITLE OF INVENTION: RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/07/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
PFIZENMAYER, MARK C	2447	714-774000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

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(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

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1 _____

2 _____

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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

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(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

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❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/246,163	10/11/2005	Marcos C. Tzannes	5550-54	5478

62574 7590 09/07/2010

Jason H. Vick
Sheridan Ross, PC
Suite # 1200
1560 Broadway
Denver, CO 80202

EXAMINER	
PFIZENMAYER, MARK C	
ART UNIT	PAPER NUMBER
2447	

DATE MAILED: 09/07/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 828 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 828 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/246,163	TZANNES ET AL.	
	Examiner	Art Unit	
	MARK PFIZENMAYER	2447	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *a telephone communications with Jason Vick (Reg. No. 45,285) on August 2 and 3, 2010*.

2. ☒ The allowed claim(s) is/are *46-53 (renumbered as claims 1-8)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/22/09 and 8/9/10
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. The applicant cancelled claims 1-45, and added claims 46-29 in the amendment filed on 12/17/2009. The applicant amended claim 46 and added claims 50-53 in the supplemental amendment filed on 12/30/2009. The applicant amended claims 46 and 50 in the supplemental amendment filed on 3/8/2010. Claims 46-53 are pending.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Authorization for this examiner's amendment was given in a telephone interviews with Jason Vick (Reg. No. 45,285) on August 2 and 3, 2010.

4. The application has been amended as follows:

- Replace claim 46 with:

46. A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

determining, at the transceiver, an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating, in the transceiver, a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for

transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

- Replace claim 47 with:

47. The method of claim 46, wherein the determining is based on an impulse noise protection requirement.

- Replace claim 48 with:

48. The method of claim 46, wherein the determining is based on a latency requirement.

- Replace claim 49 with:

49. The method of claim 46, wherein the determining is based on a bit error rate requirement.

- Replace claim 50 with:

50. A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shred memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

- Replace claim 51 with:

51. The method of claim 50, wherein the determining is based on an impulse noise protection requirement.

- Replace claim 52 with:

52. The method of claim 50, wherein the determining is based on a latency requirement.

- Replace claim 53 with:

53. The method of claim 50, wherein the determining is based on a bit error rate requirement.

Allowable Subject Matter

5. Claims 46-53 are allowed.

Claim 46 identifies the distinct features of specifying a maximum number of bytes available to be allocated to an interleaver in a transmitted or received message, determining the amount of memory required by the interleaver, and then allocating the bytes of a shared memory to the interleaver wherein the bytes allocated do not exceed the maximum number of available bytes specified in the message.

The closest prior art, Fadavi-Ardekani et al (U.S. Pat. No. 6,707,822) discloses sharing a memory between the interleavers and deinterleavers of multiple ADSL sessions, fails to suggest limiting the memory allocated to the interleaver to a maximum number of bytes available that was specified in a transmitted or received message. The above features in conjunction with all other limitations of the dependent and independent claims 46-49 are hereby allowed.

Claim 50 identifies the distinct features of specifying a maximum number of bytes available to be allocated to a deinterleaver in a transmitted or received message, determining the amount of memory required by the deinterleaver, and then allocating the bytes of a shared memory to the deinterleaver wherein the bytes allocated do not exceed the maximum number of available bytes specified in the message.

The closest prior art, Fadavi-Ardekani et al (U.S. Pat. No. 6,707,822) discloses sharing a memory between the interleavers and deinterleavers of multiple ADSL sessions, fails to suggest limiting the memory allocated to the deinterleaver to a maximum number of bytes available that was specified in a transmitted or received message. The above features in conjunction with all other limitations of the dependent and independent claims 50-53 are hereby allowed.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARK PFIZENMAYER whose telephone number is (571)270-7214. The examiner can normally be reached on Monday - Friday 8:00 - 5:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Hwang can be reached on (571)272-4036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mark Pfizenmayer
Patent Examiner
3 August 2010

/Joon H. Hwang/
Supervisory Patent Examiner, Art Unit 2447

US005751741A

United States Patent [19]

Voith et al.

[11] Patent Number: 5,751,741

[45] Date of Patent: May 12, 1998

[54] **RATE-ADAPTED COMMUNICATION SYSTEM AND METHOD FOR EFFICIENT BUFFER UTILIZATION THEREOF**

[75] Inventors: **Raymond Paul Voith; Sujit Sudhaman; George Hoekstra**, all of Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **754,768**

[22] Filed: **Nov. 20, 1996**

[51] **Int. Cl.**^{6} **H03M 13/22**

[52] **U.S. Cl.** **371/37.7**; 370/914; 371/2.2; 371/37.02

[58] **Field of Search** 371/37.02, 2.2, 371/37.7; 370/914

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,596,604	1/1997	Cioffi et al.	345/260
5,636,224	6/1997	Voith et al.	371/2.1

OTHER PUBLICATIONS

American Nat'l. Standards Institute, Inc., "Asymmetric Digital Subscriber Line (ADSL) Metallic Interface", American Nat'l. Standards Inst. Inc., Network and Customer Installation Interfaces, pp. 1–170.

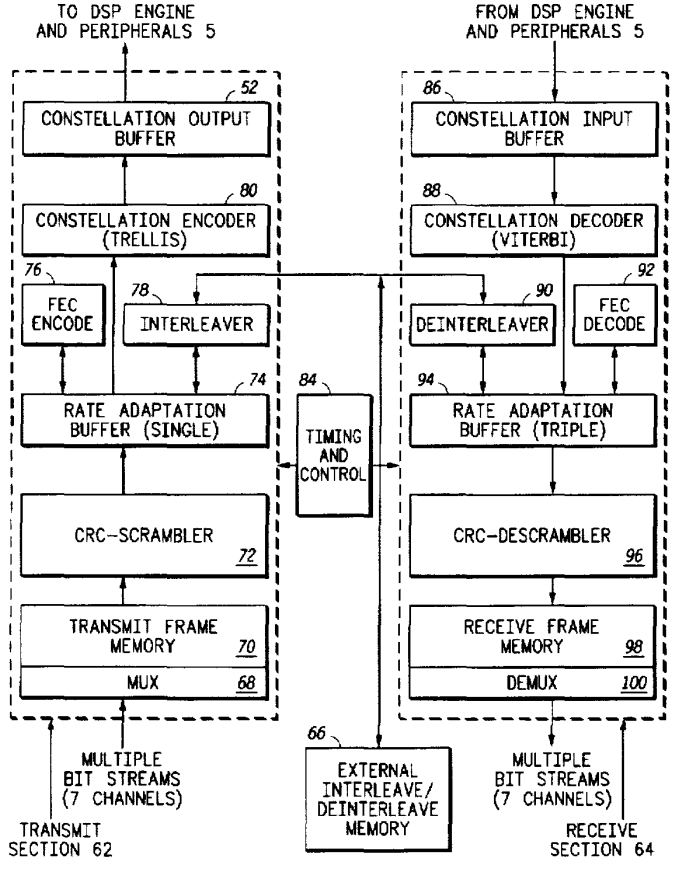
Primary Examiner—Stephen M. Baker

Attorney, Agent, or Firm—Daniel D. Hill; Paul J. Polansky

[57] **ABSTRACT**

A transceiver (**34**) includes a rate adaptation buffer (**74**) that synchronizes a data stream received at a 4.0 kHz rate to a data stream that is transmitted at a 4.05 kHz rate. A transmit section (**62**) of the transceiver (**34**) performs rate adaptation using a single rate adaptation buffer. The transmit section (**62**) includes four autonomous modules which are able to access the data in the rate adaptation buffer (**74**) independently of one another. These four modules include a CRC-scrambler (**72**), a FEC encoder (**76**), an interleaver (**78**), and a constellation encoder (**80**). A timing controller (**84**) prevents contention for accesses to the rate adaptation buffer (**74**). In addition, each of the four modules perform their respective functions quickly enough to prevent overflow or underflow conditions in the rate adaptation buffer (**74**). A receive section (**64**) functions similarly to the transmit section (**62**).

18 Claims, 6 Drawing Sheets



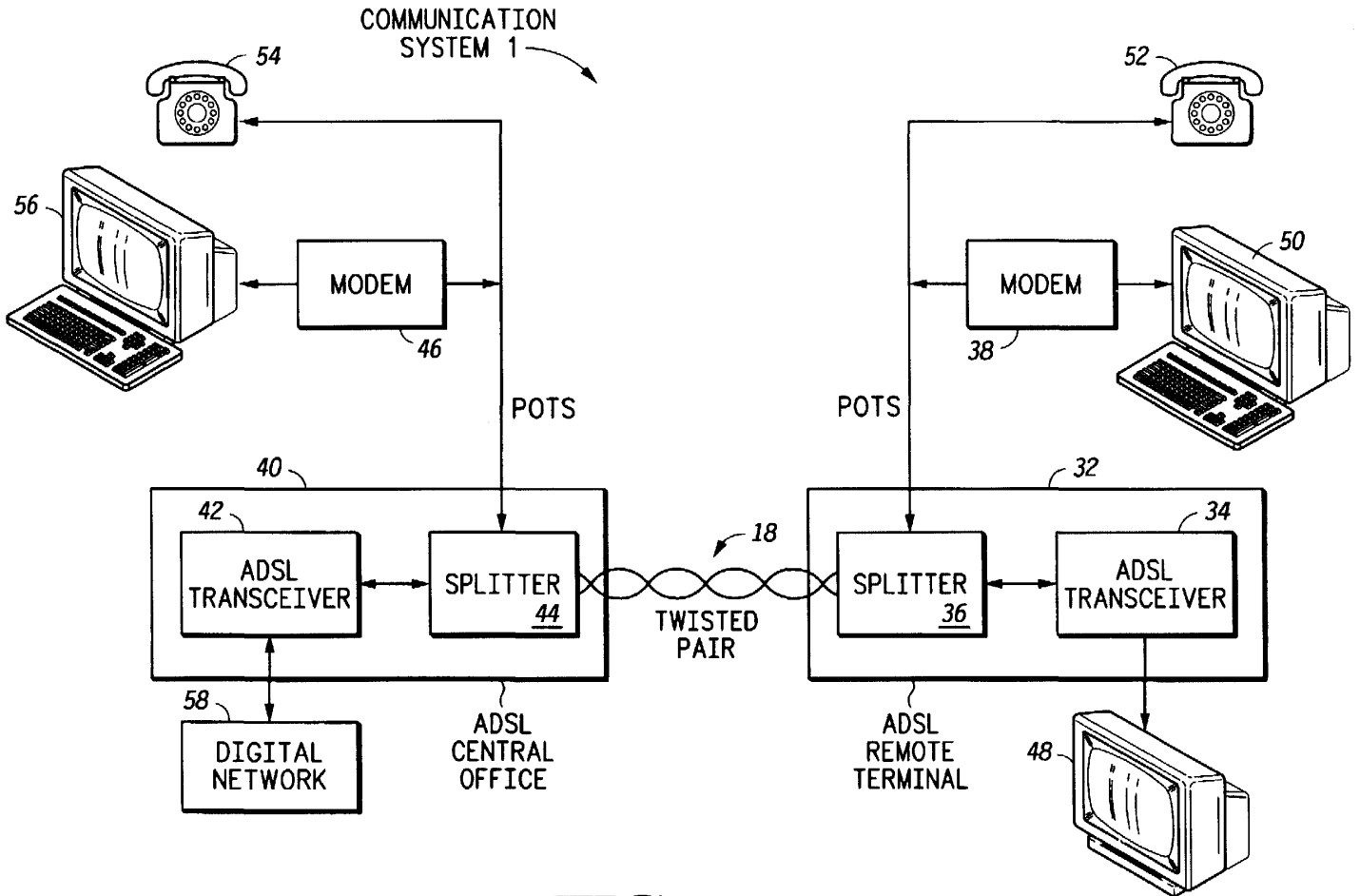

COMMUNICATION SYSTEM 1
54
52
56
MODEM
46
MODEM
38
50
POTS
POTS
40
32
42
34
ADSL TRANSCEIVER
SPLITTER 44
18
SPLITTER 36
ADSL TRANSCEIVER
TWISTED PAIR
58
DIGITAL NETWORK
ADSL CENTRAL OFFICE
ADSL REMOTE TERMINAL
48

FIG.1

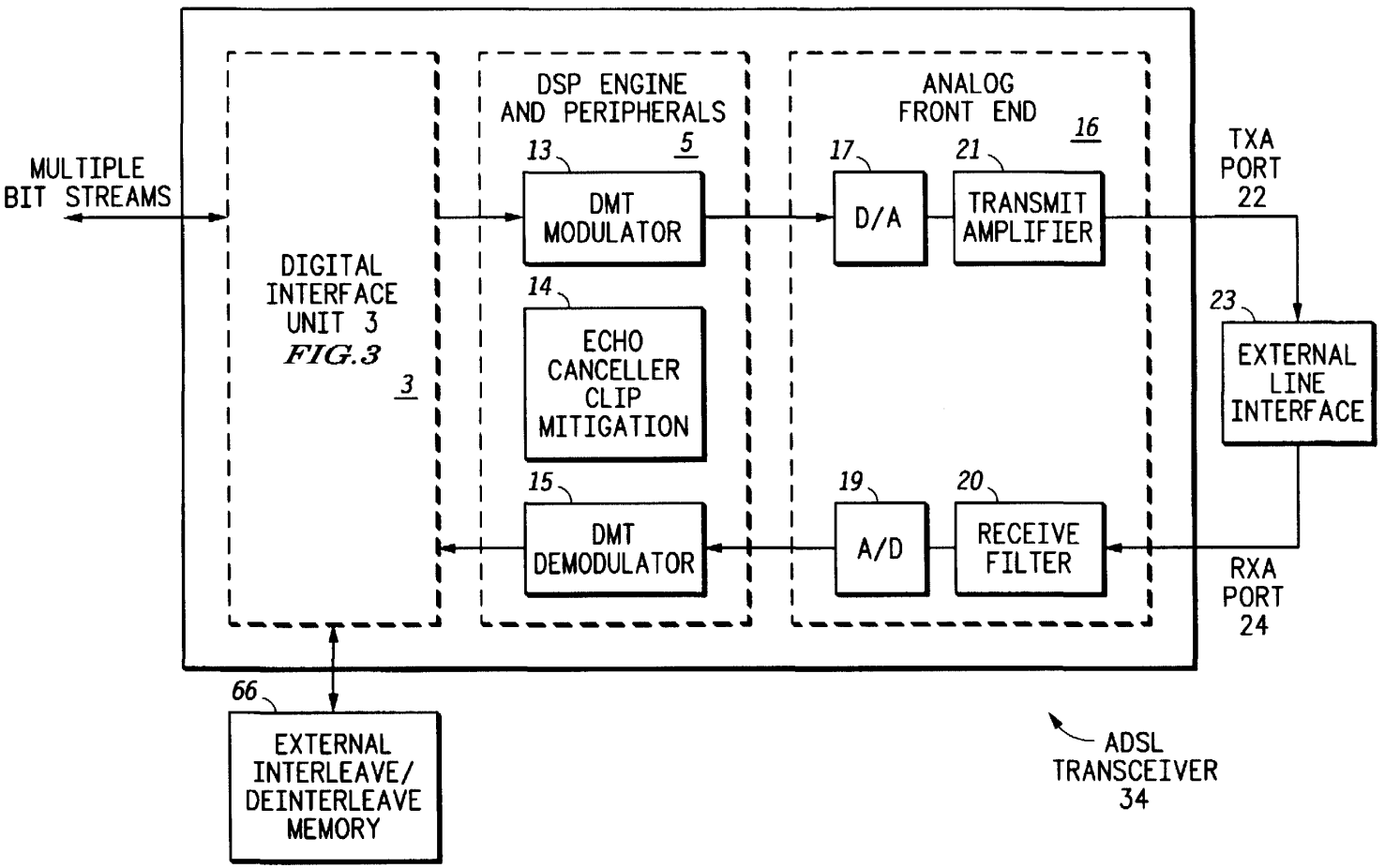

MULTIPLE BIT STREAMS
DIGITAL INTERFACE UNIT 3
3
DSP ENGINE AND PERIPHERALS
5
13
DMT MODULATOR
14
ECHO CANCELLER CLIP MITIGATION
15
DMT DEMODULATOR
ANALOG FRONT END
16
17
D/A
21
TRANSMIT AMPLIFIER
19
A/D
20
RECEIVE FILTER
TXA PORT 22
23
EXTERNAL LINE INTERFACE
RXA PORT 24
66
EXTERNAL INTERLEAVE/ DEINTERLEAVE MEMORY
ADSL TRANSCEIVER 34

FIG.3

FIG.2

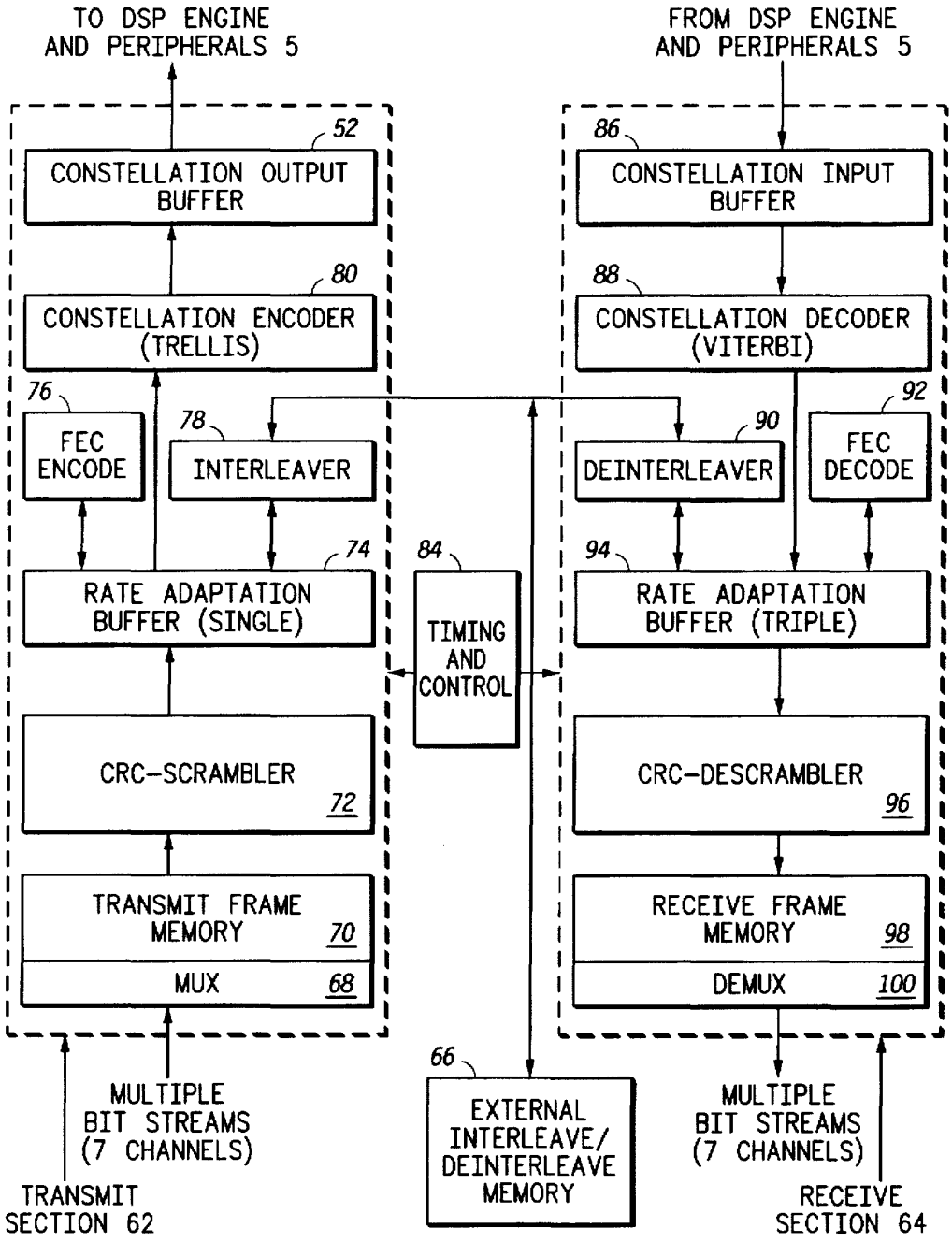

TO DSP ENGINE AND PERIPHERALS 5
FROM DSP ENGINE AND PERIPHERALS 5
52
CONSTELLATION OUTPUT BUFFER
80
CONSTELLATION ENCODER (TRELLIS)
76
FEC ENCODE
78
INTERLEAVER
74
RATE ADAPTATION BUFFER (SINGLE)
CRC-SCRAMBLER 72
TRANSMIT FRAME MEMORY 70
MUX 68
MULTIPLE BIT STREAMS (7 CHANNELS)
TRANSMIT SECTION 62
84
TIMING AND CONTROL
66
EXTERNAL INTERLEAVE/ DEINTERLEAVE MEMORY
86
CONSTELLATION INPUT BUFFER
88
CONSTELLATION DECODER (VITERBI)
90
DEINTERLEAVER
92
FEC DECODE
94
RATE ADAPTATION BUFFER (TRIPLE)
CRC-DESCRAMBLER 96
RECEIVE FRAME MEMORY 98
DEMUX 100
MULTIPLE BIT STREAMS (7 CHANNELS)
RECEIVE SECTION 64

FIG. 3

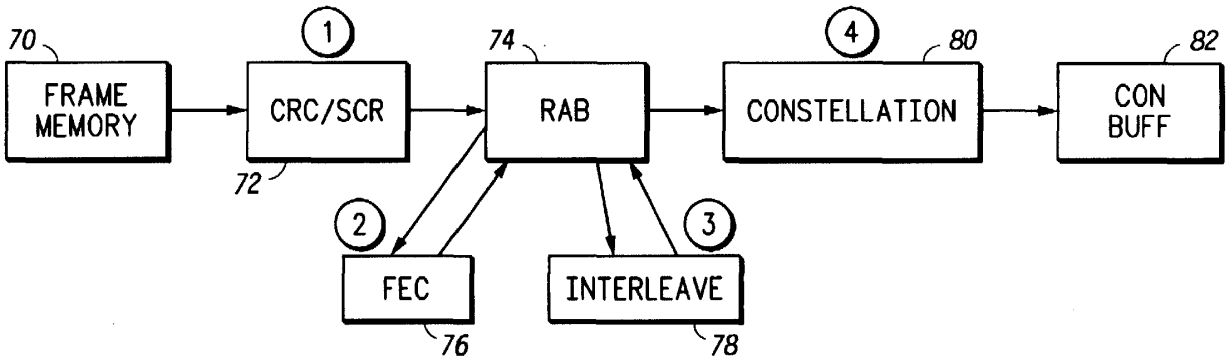

70
FRAME MEMORY
1
CRC/SCR
72
74
RAB
4
80
CONSTELLATION
82
CON BUFF
2
FEC
76
3
INTERLEAVE
78

FIG.4

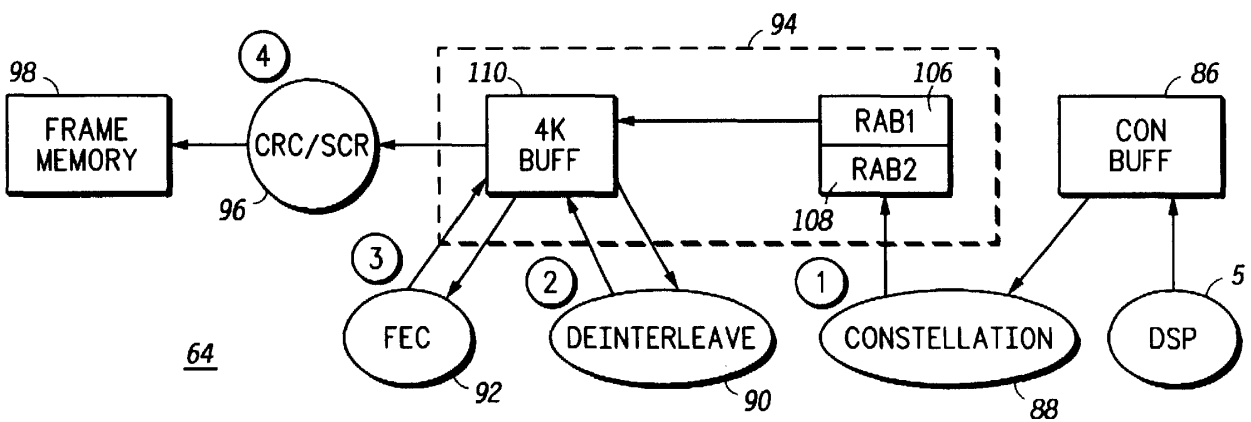

94
98
FRAME MEMORY
4
CRC/SCR
96
110
4K BUFF
106
RAB1
RAB2
108
86
CON BUFF
3
FEC
92
2
DEINTERLEAVE
90
1
CONSTELLATION
88
5
DSP
64

FIG.6

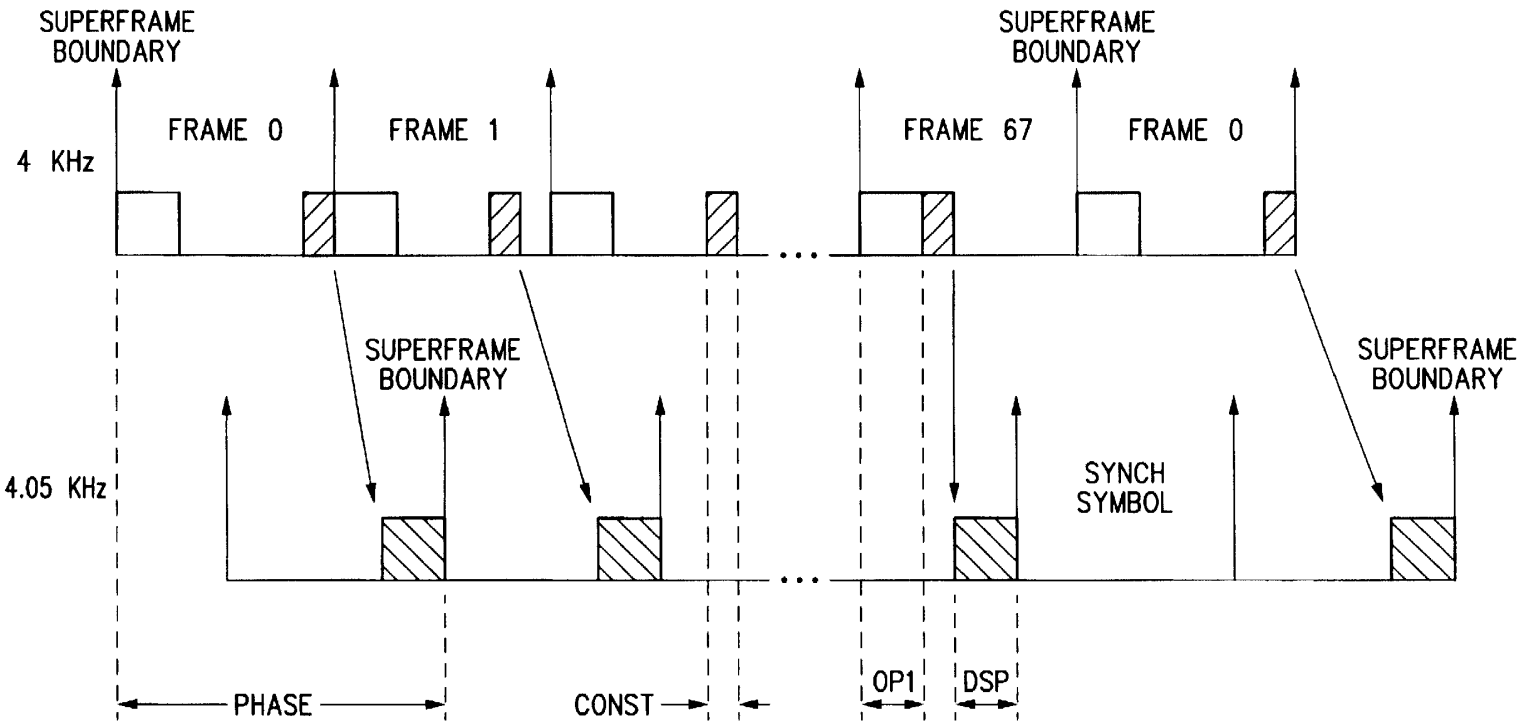

SUPERFRAME BOUNDARY
FRAME 0
FRAME 1
FRAME 67
FRAME 0
SUPERFRAME BOUNDARY
4 KHz
SUPERFRAME BOUNDARY
SUPERFRAME BOUNDARY
4.05 KHz
SYNCH SYMBOL
PHASE
CONST
OP1
DSP

FIG.5

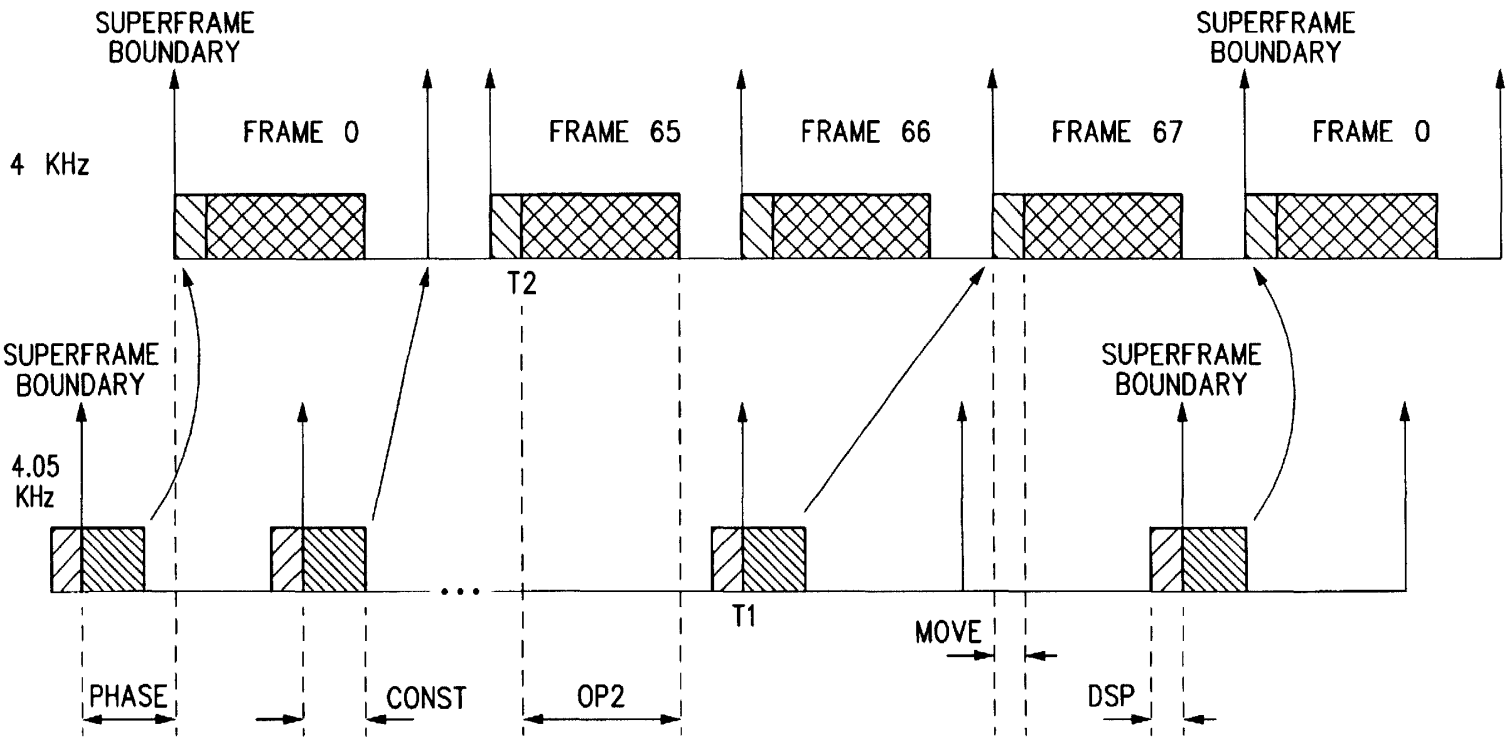

SUPERFRAME BOUNDARY
FRAME 0
FRAME 65
FRAME 66
FRAME 67
FRAME 0
SUPERFRAME BOUNDARY
4 KHz
T2
SUPERFRAME BOUNDARY
SUPERFRAME BOUNDARY
4.05 KHz
T1
MOVE
PHASE
CONST
OP2
DSP

FIG. 7

RATE-ADAPTED COMMUNICATION SYSTEM AND METHOD FOR EFFICIENT BUFFER UTILIZATION THEREOF

FIELD OF THE INVENTION

This invention relates generally to communications, and more particularly, to communications systems requiring rate adaptation.

BACKGROUND OF THE INVENTION

As the complexity of communication systems increases, there is more and more need for additional ways of transmitting information. One method of communication is called Asymmetrical Digital Subscriber Line (ADSL) and is a transmission scheme that allows for the provision of plain old telephone service (POTS) and a variety of digital channels on two wire twisted metallic wire pair with mixed gauges. It is desirable to use such twisted pair wire as there is an existing infrastructure, the use of which will reduce installation costs. ADSL standards are proposed in the draft American National Standard for Telecommunication—Network and Customer Interfaces—Asymmetric Digital Subscriber Line (ADSL) metallic interface, T1E1.4/95-007R2, ADSL coding standard, draft, Aug. 15, 1995.

Discrete multi-tone (DMT) is a multi-carrier technique which divides the available bandwidth of twisted-pair copper media connections into mini-subchannels or bins. The DMT technique has been proposed for adoption by the ANSI T1E1.4 (ADSL) committee to be used in ADSL communications systems. In the proposed ADSL standard, T1E1.4 DMT is used to generate 250 separate 4.3125 kilohertz (kHz) subchannels from 26 kilohertz to 1.1 megahertz (MHz) for downstream transmission to an end user. Likewise, DMT is used to generate 26 subchannels from 26 kilohertz to 138 kilohertz for upstream transmission by an end user. The asymmetric transmission protocol implemented by the proposed ADSL standard requires a higher rate of data transmission from a central office to a remote terminal and a lower rate of data transmission from a remote terminal to a central office. As a result, different processing sequences are required at the remote terminal and central office ends.

One of the advantages of ADSL transmission is that it may be used to provide high quality, multiple and simultaneous interactive video services over an ordinary telephone line without disruption of the standard telephone service.

In ADSL, data may be received from (and provided to) several channels and the data is grouped into structures known as frames. Each frame includes both payload data bytes and overhead bytes. Data from each channel is placed in different positions in the frame depending on whether it is interleaved or non-interleaved. In general, for transmission, the ADSL equipment must assemble the payload data from the channels into a frame and append the overhead bytes as appropriate. In particular, the ADSL equipment must perform a cyclic redundancy check (CRC), scramble, interleave (if selected), and perform forward error correction coding (FEC) on frame data. Once the transmit data and overhead bytes are assembled into a frame, the ADSL equipment must convert the frame data into a set of complex symbols. Each symbol represents a number of frame bits as defined by a bit allocation table. These complex symbols are subsequently converted into an analog signal transmitted on the telephone line. Conversely, when receiving an analog signal from the telephone line, the ADSL equipment must convert the analog signal into complex digital symbols, convert the complex symbols into a receive frame, and perform deinterleaving, FEC, CRC, and descrambling to convert the received frame into recovered payload data.

The frames in turn are grouped together into a "superframe" which includes 68 data frames plus an additional synchronization frame. CRC calculation is performed on all the data in the 68 data frames of a superframe, and the CRC calculated for a prior superframe is transmitted in the overhead bytes of the first frame of the next superframe. The synchronization frame is a special frame which the ADSL equipment uses to delineate the boundary of a superframe.

The existence of the synchronization frame creates a rate adaptation problem with the ADSL equipment. On the transmit side, 68 frames of transmit data are gathered in 17 milliseconds (ms), but symbols corresponding to 69 frames (68 frames plus the synchronization frame) are transmitted on the telephone line in the same amount of time. Similarly on the receive side, symbols corresponding to 69 frames of receive data (68 frames plus the synchronization frame) are received from the telephone line in 17 microseconds but only 68 frames are processed in the same amount of time. One way of solving this problem is to add a large buffer area so that while the supplier of data is filling one part of the buffer from one side, the consumer of data is emptying another part of buffer from the other side. However, large buffers consume a large integrated circuit area which adds to its cost. Another problem is that the ADSL equipment must perform all the functions required quickly enough to avoid overflow and underflow conditions. The present invention overcomes these problems by providing an efficient ADSL apparatus, whose features and advantages will be more clearly understood by reference to the Detailed Description in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates, in block diagram form, an asymmetrical digital subscriber line (ADSL) communication system in accordance with one embodiment of the present invention.

FIG. **2** illustrates, in block diagram form, the ADSL transceiver of FIG. **1**.

FIG. **3** illustrates, in block diagram form, the digital interface of FIG. **2**.

FIG. **4** illustrates, in block diagram form, the signal processing operations performed on the transmit rate adaptation buffer of FIG. **3**.

FIG. **5** illustrates a timing diagram of the signal processing operations performed on the transmit rate adaptation buffer of FIG. **3**.

FIG. **6** illustrates, in block diagram form, the signal processing operations performed on the receive rate adaptation buffer of FIG. **3**.

FIG. **7** illustrates a timing diagram of the signal processing operations performed on the receive rate adaptation buffer of FIG. **3**.

DESCRIPTION OF A PREFERRED EMBODIMENT

Generally, the present invention provides an ADSL transceiver having a rate adaptation buffer that synchronizes a data stream received at a 4.0 kHz rate to a data stream that is transmitted at a 4.05 kHz rate. A transmit section of the transceiver is able to perform this rate adaptation using a single rate adaptation buffer, without the need for multiple frame buffering as in known rate adaptation techniques. The

transmit section includes four autonomous modules which are able to access the data in the rate adaptation buffer independently of one another. These four modules include a CRC-scrambler, a FEC encoder, an interleaver, and a constellation encoder. Timing control prevents contention for accesses to the rate adaptation buffer. In addition, each of the four modules perform their respective functions quickly enough to prevent overflow or underflow conditions in the rate adaptation buffer.

In a receive section of the transceiver, rate adaptation is performed in a manner similar to that of the transmit section, except that there are stricter timing constraints. Because some of the receive processing tasks cannot be completed until the whole frame is available, the receive section requires a minimum of three rate adaptation buffers. Similarly to the transmit section, four modules in the receive section are each independent from each other in the sense that they are all able to address the rate adaptation buffer. The four modules include a deinterleaver, an FEC decoder, a CRC-descrambler, and a constellation decoder. A timing and control section prevents contention between the four modules.

This allows the synchronization of the 4.0 kHz rate of a superframe having 68 frames to the 4.05 kHz rate of a superframe having 69 frames (68 payload frames plus a synchronization frame) without using a large amount of memory. Thus, the size and cost required to implement the ADSL transceiver is reduced.

FIG. **1** illustrates a communication system **1**, according to one embodiment of the present invention, having an ADSL remote terminal **32** and an ADSL central office **40**. ADSL central office **40** contains ADSL transceiver **42** and splitter **44**. ADSL central office **40** is coupled to ADSL remote terminal **32** by way of twisted pair **18**. ADSL remote terminal **32** includes splitter **36** and ADSL transceiver **34**.

ADSL transceiver **42** is bi-directionally coupled to splitter **44**, and is additionally bi-directionally coupled externally to digital network **58**. ADSL transceiver **34** is bi-directionally coupled to splitter **36**, and is additionally coupled to external devices **48**. Splitter **44** is bi-directionally coupled to telephone **54**, while splitter **36** is bi-directionally coupled to telephone **52**. Splitter **44** is additionally coupled to modem **46** and splitter **36** is coupled to modem **38**. Modem **38** is further coupled to external terminals **50** and modem **46** is coupled to external terminals **56**.

Communication system **1** is an example of a digital communication network, where the digital network allows communication between a variety of users having computers, telephones, fax machines, modems, television sets, and any number of other communication devices. Digital network **58** is used to transmit such a variety of information, each of which has a different transmission format and frequency.

FIG. **2** illustrates ADSL transceiver **34** of FIG. **1**, along with an external interleave/de-interleave memory **66**. Here, ADSL transceiver **34** may be a single chip embodiment and is substantially the same as ADSL transceiver **42**. Referring to FIG. **2**, ADSL transceiver **34** includes digital interface unit **3**, which is coupled to digital signal processing (DSP) engine and peripherals **5**. Further, DSP engine and peripherals **5** is coupled to analog front end **16**. Digital interface unit **3** is bi-directionally coupled to receive signals labeled "MULTIPLE BIT STREAMS", and is bi-directionally coupled to an external interleave/deinterleave memory **66**.

Analog front end **16** contains analog/digital converter (A/D) **19** which is coupled to receive filter **20**. Analog front end **16** further includes transmit amplifier **21** which is coupled to digital/analog converter (D/A) **17**. Transmit amplifier **21** is further coupled to TXA port **22**. Receive filter **20** is coupled to port **24**. RXA port **22** is then coupled to external line interface **23**. External line interface **23** is coupled to both ports **22** and **24**.

DSP engine and peripherals **5** includes a digital signal processor and firmware necessary to perform various signal processing functions. These functions include a DMT modulator **13**, an echo canceller clip mitigation **14**, and a DMT demodulator as illustrated in FIG. **2**. DMT modulator **13** has an input coupled to digital interface unit **3**, and an output coupled to D/A converter **17**. DMT demodulator **15** has an input coupled to A/D converter **19**, and an output coupled to digital interface unit **3**. Echo cancellation clip mitigation **14** is an additional signal processing function performed by DSP engine and peripherals **5**, and these functions are performed on both the transmit and receive sides by subtracting echo terms of one path from the signal in the other path.

Digital interface unit **3** includes a bidirectional port for receiving and transmitting payload data, which is labeled "MULTIPLE BIT STREAMS" in FIG. **2**. When receiving data for transmission, digital interface unit **3** receives transmit payload data from the MULTIPLE BIT STREAMS and outputs sets of complex symbols to DMT modulator **13**. Similarly, digital interface unit **3** receives sets of complex symbols from DMT demodulator **15** and outputs receive payload data to the MULTIPLE BIT STREAMS. As part of the ADSL task, digital interface unit **3** also interleaves transmit data and de-interleaves receive data. In order to perform these complex functions, ADSL transceiver **34** requires a large amount of memory, which is preferably implemented off-chip in external interleave/de-interleave memory **66**. Also, in order to minimize the number of integrated circuit pins required to access external memory, the interleave and de-interleave buffers are also preferably implemented in the same physical memory and digital interface unit **3** preferably multiplexes between interleaving and de-interleaving operations.

The operation of digital interface unit **3** is understood with reference to FIG. **3**, which illustrates digital interface unit **3** in block diagram form. Digital interface unit **3** generally includes a transmit section **62**, a receive section **64**, and common timing and control portion **84** which coordinates the operation between the two sections. Also illustrated in FIG. **3** is an external interleave/de-interleave memory **66**, which is used by both transmit section **62** and receive section **64**.

Timing control block **84** generates timing signals which are necessary for the signal processing functions. Timing control block **84** also coordinates the activities of several modules in both the transmit and receive path so that their activities do not conflict. Furthermore, timing control block **84** includes a memory arbitrator that arbitrates between the transmit and receive path for access to external interleave/deinterleave memory **66**.

The operation of digital interface unit **3** is better understood first by examining transmit section **62**. Transmit section **62** includes a multiplexer (MUX) **68**, a transmit frame memory **70**, a CRC-scrambler **72**, a rate adaptation buffer **74**, an FEC encode block **76**, an interleaver **78**, a constellation encoder **80**, and a constellation output buffer **82**. MUX **68** has an input for receiving the MULTIPLE BIT STREAMS and is coupled to transmit frame memory **70**. Transmit frame memory **70** has an input coupled to MUX

68, and an output. CRC-scrambler 72 has an input connected to transmit frame memory 70, and an output. Rate adaptation buffer 74 has an input connected to the output of CRC-scrambler 72, two bi-directional connections to FEC encode 76 and interleaver 78, and an output connected to constellation encoder 80. Interleaver 78 also has a second bidirectional terminal connected to external interleave/deinterleave memory 66. Constellation encoder 80 has an input terminal connected to rate adaptation buffer 74, and an output connected to constellation output buffer 82. Constellation output buffer 82 has an output which is connected to DSP engine and peripherals 5 of FIG. 2.

Receive section 64 includes generally a constellation input buffer 86, a constellation decoder 88, a de-interleaver 90, an FEC decode 92, a rate adaptation buffer 94, a CRC-descrambler 96, a receive frame memory 98, and a demultiplexer (DEMUX) 100. Constellation input buffer 86 has an input connected to DSP engine and peripherals 5 of FIG. 2, and an output. Constellation decoder 88 has an input connected to the output of constellation input buffer 86, and an output. De-interleaver 90 has a first bidirectional terminal, and a second bidirectional terminal connected to external interleave/deinterleave memory 66. FEC decode 92 has a bidirectional terminal. Rate adaptation buffer 94 has an input terminal connected to the output terminal of constellation decoder 88, a first bi-directional terminal connected to the bi-directional terminal of deinterleaver 90, a second bidirectional terminal connected to the bi-directional terminal of FEC decode 92, and an output terminal. CRC-descrambler 96 has an input terminal connected to the output terminal of rate adaptation buffer 94, and an output terminal. Receive frame memory 98 has an input terminal connected to the output terminal of CRC-descrambler 96, and an output terminal connected to an input terminal of DEMUX 100. DEMUX 100 also has an output terminal which provides seven channels of data to the MULTIPLE BIT STREAMS. External interleave/deinterleave memory 66 has a bidirectional terminal coupled to the second bidirectional terminals of interleaver 78 and deinterleaver 90.

In operation, MUX 68 receives MULTIPLE BIT STREAMS which may be organized into a maximum of seven channels. Note that some of the channels need not be present in a particular application. These seven channels of payload data are then stored in corresponding portions of transmit frame memory 70. In addition, transmit frame memory 70 appends a FAST byte and a SYNC byte, defined by the ADSL standard, at the appropriate points in the frame. CRC-scrambler 72 then reads the corresponding portions of the frame from transmit frame memory 70. CRC-scrambler 72 performs an 8-bit cyclic redundancy check first on the fast data and then on the interleaved data. The scrambler function of CRC-scrambler 72 also operates first on the fast data and next on the interleaved data. CRC-scrambler 72 makes the modified transmit frame available to other signal processing blocks by writing it into rate adaptation buffer 74. In the illustrated embodiment, rate adaptation buffer 74 comprises a single static random access memory (SRAM).

FEC encode 76 performs a forward error correction encoding first on fast data and next on the interleaved data in the frame and appends redundancy bytes to the frame and stores those in appropriate portions of rate adaptation buffer 74. Interleaver 78 operates only on the interleave portion of the frame, and reads data out of rate adaptation buffer 74 and writes data back into rate adaptation buffer 74 after performing the interleaving operation. Because the interleaving operation requires a large amount of memory, interleaver 78 uses a portion of external interleave/deinterleave memory 66. Interleaver 78 arbitrates for use of external interleave/deinterleave memory 66 with deinterleaver 90 so that only one external memory interface using common integrated circuit pins is required. At the conclusion of the CRC-scrambling FEC encoding and interleaving operations, constellation encoder 80 reads data from rate adaptation buffer 74. Constellation encoder 80 encodes the data into complex symbols based on a bit allocation table, and may use the well-known trellis encoding method. The bit allocation table is determined at initialization between the central office and the remote terminal based on the characteristics of the transmission link. Constellation encoder 80 then provides the complex symbols to constellation output buffer 82 for further processing by DSP engine and peripherals 5.

In receive section 64, data in the form of sets of complex symbols are received from DSP engine and peripherals 5 which writes them into constellation input buffer 86. Constellation decoder 88 reads the complex symbols from constellation input buffer 86 and converts them into frame data based on a bit allocation table. In the illustrated embodiment, constellation decoder 88 includes the well-known Viterbi algorithm as an option. Note that other algorithms may also be used. Constellation decoder 88 then writes the frame data into rate adaptation buffer 94. A deinterleaver 90 performs a deinterleave operation on the interleaved portion of the received frame. Deinterleaver 90 makes use of external interleave/deinterleave memory 66 and arbitrates for usage thereof in a manner similar to interleaver 78. FEC decode 92 first performs an FEC decode operation on the fast portion of the frame data, and then performs an FEC decode operation on the interleaved portion of the frame data. If FEC decode 92 detects an error in the frame data, it performs correction within rate adaptation buffer 94. CRC-descrambler 96 reads the completed frame data out of rate adaptation buffer 94. CRC-descrambler 96 descrambles the frame data by first operating on the fast data and next on the interleaved data as well. CRC-descrambler 96 performs a CRC check on the fast data and next on the interleave data. CRC-descrambler 96 then writes the data into receive frame memory 98. The data in receive frame memory 98 is then output to the corresponding channel selected by DEMUX 100, which become part of the MULTIPLE BIT STREAMS.

Transmit section 62 is able to perform rate adaptation by receiving data at a 4 kilohertz rate from the MULTIPLE BIT STREAMS and providing data out of constellation output buffer 80 at a rate of 4.05 kilohertz for the frame. Transmit section 62 is able to perform this rate adaptation using only a single rate adaptation buffer 74 and without the need for multiple frame buffering as in known rate adaptation techniques. Transmit section 62 includes four autonomous modules which are able to access the data in rate adaptation buffer 74 independently of one another. These four modules include CRC-scrambler 72, FEC encoder 76, interleaver 78, and constellation encoder 80. Note that timing control 84 prevents contention for accesses to rate adaptation buffer 74. In addition, each of the four independent modules perform their respective functions quickly enough to prevent overflow or underflow conditions in rate adaptation buffer 74. The speed of these operations is facilitated by the use of independent modules which may each independently access rate adaptation buffer 74. As described herein, the term "independent" means that each module is capable of independently addressing needed data in rate adaptation buffer 74. However, timing and control 84 insures that there is no contention between the modules by allowing access to rate adaptation buffer 74 in a time sharing sense. The necessity

of storing or receiving data at a four kilohertz frame rate and providing data at a 4.05 kilohertz rates creates constraints in the timing and sequence of operations of the various modules of transmit section **62**. These timing constraints will be better understood with reference to both FIGS. **4** and **5**.

In receive section **64** the rate adaptation problem is similar to that of the transmit side except there are stricter timing constraints. In the case of receive section **64**, data is being provided from DSP and peripherals **5** at a rate of 4.05 kilohertz per frame into constellation input buffer **86**. Because some of the receive processing tasks cannot be completed until the whole frame is available, receive section **64** requires a minimum of three frame buffers. Similarly to transmit section **62**, in receive section **64**, the four modules are each independent in the sense that they are all able to address rate adaptation buffer **64**. But again, timing and control **84** must prevent contention. In addition, timing and control **84** must transfer data between the three frame buffers when particular signal processing functions have completed. These additional constraints will be better understood with reference to FIGS. **6** and **7** below.

FIG. **4** illustrates, in block diagram form, the functions performed by transmit section **62**. FIG. **4** is useful in understanding the sequence of operations provided on data in transmit section **62**. This sequence of processing will become helpful in the understanding of the timing constraints which will be explored further with reference to FIG. **5** below. In FIG. **4** proceeding from left to right, data is first assembled into frame memory **70**. Note that elements in FIG. **4** which are in common with FIG. **3** are assigned the same reference numbers. CRC-scrambler **72** represents the first operation performed on data with reference to rate adaptation buffer **74**. CRC-scrambler **72** reads data out of frame memory **70** and writes data into rate adaptation buffer **74**. An FEC encode operation represents the second operation performed on the data in rate adaptation buffer **74**. To perform FEC encoding, FEC encoder **76** first reads data out of rate adaptation buffer **74** and later writes data back into rate adaptation buffer **74**. The interleave operation is performed by interleaver **78** and represents the third operation. In this third operation, interleaver **78** also reads data out of rate adaptation buffer **74** and subsequently writes data back into rate adaptation buffer **74**. The fourth operation associated with transmit section **62** is that performed by constellation encoder **80**. In performing this function, constellation encoder **80** reads data out of rate adaptation buffer **74** and converts the data into sets of complex signals. The complex symbols are not rewritten into rate adaptation buffer **74**, but rather are written to constellation output buffer **82**.

This sequence is used for understanding the timing constraints which are developed in FIG. **5**, which illustrates a timing diagram of the transmission of a superframe of data. In FIG. **5** the upper most timing axis represents a superframe of data to be transmitted which is received at a 4 kilohertz rate. Within the superframe there are 68 frames labeled frame **0**, frame **1**, etc. through frames **67**. Following frame **67** is a frame **0** of a succeeding frame. The time point between frame **67** and frame **0** of the next frame represents a superframe boundary. The second horizontal axis represents the reading of frames by DSP engine and peripherals **5** at the higher rate of 4.05 kilohertz. Note that there are 69 frames number **0** through **68** in the 4.05 kHz superframe. By examining the time that the four signal processing functions of FIG. **4** require, it is possible to determine a time interval labeled "PHASE" which allows transmit section **62** to synchronize the 4 kHz rate to the 4.05 kHz rate. Setting this phase value consistent with various timing constraints allows 68 frames to be received for transmission in the same amount of time that 69 frames are transmitted on a telephone line without requiring more than one frame buffer of memory in rate adaptation buffer **74**.

As illustrated in FIG. **5**, the PHASE value represents the difference in time between the start of a superframe received at the 4 kilohertz rate and the start of transmission of the same superframe at the 4.05 kilohertz rate. Note that FIG. **5** illustrates three other variables which relate to timing constraints as will be further described below. The first variable is an interval labeled "CONST" which represents the amount of time it takes constellation encoder **82** to compute the set of complex symbols for one frame of data. A second value labeled "OP1" represents the amount of time required for operations one, two and three as illustrated in FIG. **4**. Finally, the interval labeled "DSP" represents the amount of time it takes DSP and peripherals **5** to read the contents of constellation output buffer **82**.

FIG. **6** illustrates, in block diagram form, the signal processing functions performed on data which is stored in rate adaptation buffer **94**. As before, functions which are like those performed in FIG. **3** are assigned the same reference numbers. Note that as illustrated in FIG. **6**, rate adaptation buffer **94** includes a first buffer **106** labeled "RAB1", a second buffer **108** labeled "RAB2" and a third 4 kHz buffer **110**. Note that in FIG. **6** the sequence of operations proceeds right to left. First, DSP and peripherals **5** provide data to constellation buffer **86** at a frame rate of 4.05 kilohertz. A constellation decoder **88** then reads data from constellation buffer **86** to perform a first function and writes the data into one of RAB1 or RAB2 which are used in an alternating fashion. When constellation decoder **88** completes processing of a frame of data that frame of data is then transferred into 4 kHz buffer **110** at an appropriate time. In the illustrated embodiment, the 4 kHz buffer is an SRAM array. At this point, constellation decoder **88** starts the use of another one of RAB1 and RAB2 for the next frame. RAB1 and RAB2 are portions of a single SRAM array. This second operation by receive section **64** is the deinterleave operation **2** performed by deinterleaver **90**. The deinterleave operation is performed by reading data from 4 kilohertz buffer **110** and writing data back into 4 kHz buffer **110**. The third operation is the FEC decoding provided by FEC decode **92**. Likewise, FEC decode **92** reads data from 4 kHz buffer **110** and writes data back into 4 kHz buffer **110**. Finally, the fourth operation performed by receiver section **60** is a CRC-descrambling operation performed by CRC-descrambler **96**. To perform this operation, CRC-descrambler **96** reads data out of 4 kHz buffer **110** and writes the descrambled data into frame memory **98**. Note that since constellation decoder **88** must operate for an entire frame period, the receive operation is necessarily more difficult in terms of buffering than the transmit operation. In addition, the data provider is working at a faster rate and therefore will of necessity provide more data than can be handled at the slower rate. Thus, constellation decoding is performed independently on data in a different buffer from the other three operations and an additional frame buffer is required to allow storing the overflowing data arriving at the faster 4.05 kHz rate.

FIG. **7** illustrates a timing diagram of the various events associated with receive section **64** which are helpful in understanding the timing constraints imposed by the various events. The first horizontal axis represents the sequence of frames received and provided to the multiple bit streams at the 4 kilohertz rate. As in FIG. **5** there are 68 frames of a superframe and individual frames in the superframe are illustrated including a superframe boundary between frame

67 and frame 0 of a subsequent superframe. The second horizontal axis represents frames received from DSP and peripherals 5 through constellation buffer 86 at the 4.05 kilohertz rate. Also, in FIG. 7 are several time durations which represent constraints imposed on the sequence of events. The first variable labeled "PHASE" is the delay between the start of the 4.05 kilohertz super frame and the start of the 4 kilohertz super frame. The second variable is labeled "CONST" and represents the period of time required for constellation decoder 88 to convert the set of symbols into constellation buffer 86 into a frame of data. A third variable labeled OP2 represents the amount of time required for the deinterleaving, FEC decoding, and CRC-descrambling operations. A fourth variable labeled MOVE represents the amount of time it takes to move a frame of data from a full one of RAB1 or RAB2 into 4 kHz buffer 110. A fifth variable labeled "DSP" represents the amount of time required by DSP and peripherals 5 to write a set of symbols into constellation buffer 86 which corresponds to a complete frame of data. In addition, FIG. 7 illustrates two time points which also form constraints.

A point in time labeled "T1" is the point in time at which the received data corresponding to frame 67 is being written into either RAB1 or RAB2. A point in time labeled "T2" is the time when a MOVE operation is completed from either RAB1 or RAB2 into the 4 kHz buffer in order to accommodate the write of received data corresponding to frame 67 into RAB1 or RAB2.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

What is claimed is:

1. An asymmetric digital subscriber line (ADSL) transmitter, comprising:

a transmit frame memory for receiving a bit stream at a first rate, and storing the bit stream as a frame of data;

a cyclic redundancy check (CRC) scrambler, coupled to the transmit frame memory, for operating on the frame of data;

a forward error correction encoder, for performing an encoding operation on the frame of data;

an interleaver, for selectively interleaving at least a portion of the frame of data;

a rate adaptation buffer, coupled to the CRC-scrambler, the forward error correction encoder, and the interleaver, the rate adaptation buffer for temporarily storing the frame of data after the forward error correction encoder, the interleaver, and the CRC-scrambler operate on the frame of data to provided a modified frame of data; and

an encoder, coupled to the rate adaptation buffer, for providing a new frame of data at a second rate different from the first rate.

2. The ADSL transmitter of claim 1, wherein the rate adaptation buffer consists of only a single random access memory.

3. The ADSL transmitter of claim 1, wherein the encoder is characterized as being a constellation encoder.

4. The ADSL transmitter of claim 1, wherein the rate adaptation buffer is for temporarily storing the frame of data for an amount of time required for the encoder to transmit a previous frame of data.

5. A method for transmitting a frame of data in a communication system, the method comprising the steps of:

receiving the frame of data, at a first rate, in a frame memory;

performing at least two operations on the frame of data to produce a modified frame of data, and moving the modified frame of data to a rate adaptation buffer after each of the at least two operations; and

providing the modified frame of data to an output buffer, the output buffer providing a buffered frame of data at a second rate different from the first rate.

6. The method of claim 5, wherein the step of performing the at least two operations further comprises the steps of:

performing a cyclic redundancy check (CRC) scrambling operation on the frame of data to produce a scrambled frame of data;

providing the scrambled frame of data to the rate adaptation buffer;

performing an encoding operation on the scrambled frame of data to produce a encoded scrambled frame of data;

providing the encoded scrambled frame of data to the rate adaptation buffer; and

performing an interleaving operation on at least a portion of the encoded scrambled frame of data to produce an interleaved encoded scrambled frame of data.

7. The method of claim 6, further comprising the steps of:

providing the interleaved encoded scrambled frame of data to the rate adaptation buffer; and

performing a constellation encoding operation of the interleaved encoded scrambled frame of data to produce the buffered frame of data.

8. The method of claim 7, wherein the rate adaptation buffer is cleared by the constellation encoding operation before the scrambled frame of data can be received.

9. The method of claim 7, wherein the output buffer is cleared before the constellation encoding operation is performed.

10. An asymmetric digital subscriber line (ADSL) receiver, comprising:

a constellation decoder for receiving a frame of data at a first rate and providing a decoded frame of data;

a rate adaptation buffer, coupled to the constellation decoder, for temporarily storing the decoded frame of data;

a forward error correction decoder, coupled to the rate adaptation buffer, for decoding the frame of data;

a deinterleaver, coupled to the rate adaptation buffer, for deinterleaving an interleaved portion of the frame of data;

a cyclic redundancy check (CRC) descrambler, coupled to the rate adaptation buffer, for descrambling the frame of data to produce a descrambled frame of data; and

a receive frame memory, coupled to the descrambler, for receiving the descrambled frame of data at a second rate, the second rate being different than the first rate.

11. The ADSL receiver of claim 10, wherein the rate adaptation buffer comprises first, second, and third portions, wherein the first and second portions alternately receive decoded frames of data from the constellation decoder, the third portion coupled to both the first and second portions and alternately receives the decoded frames of data from the first and second portions on a first in, first out basis, the third portion coupled to the CRC-descrambler, the deinterleaver, and the forward error correction decoder.

12. The ADSL receiver of claim 10, further comprises an input buffer for receiving a plurality of frames of data and coupled to the constellation decoder.

13. The ADSL receiver of claim 10, wherein the rate adaptation buffer is for temporarily storing at least one frame of data that has arrived at the rate adaptation buffer before the at least one frame of data can be operated on by the CRC-descrambler, the deinterleaver, and the forward error correction decoder.

14. A method for receiving a frame of data in a communication system, the method comprising the steps of:

receiving the frame of data, at a first rate, in an input buffer;

decoding the frame of data and providing a decoded frame of data to a rate adaptation buffer;

performing at least two operations on the frame of data to produce a modified frame of data, and moving the modified frame of data to the rate adaptation buffer after each of the at least two operations; and

providing the modified frame of data to a receive frame memory, the receive frame memory providing the modified frame of data at a second rate different from the first rate.

15. The method of claim 14, further comprising a step of descrambling the modified frame of data before the step of providing the modified frame of data to the receive frame memory.

16. The method of claim 14, wherein the step of performing the at least two operations further comprises the steps of:

providing a decoded frame of data to one of a first portion or a second portion of the rate adaptation buffer;

moving the decoded frame of data to a third portion of the rate adaptation buffer from the first or the second portion;

performing a deinterleaving operation on at least a portion of the decoded frame of data to produce a deinterleaved decoded frame of data;

providing the deinterleaved decoded frame of data to third portion of the rate adaptation buffer;

performing a forward error correction decoding operation on the deinterleaved decoded frame of data to produce a decoded deinterleaved frame of data;

providing the deinterleaved decoded frame of data to the third portion of the rate adaptation buffer; and

performing a cyclic redundancy check (CRC) descrambling operation on the deinterleaved decoded frame of data to produce a descrambled frame of data.

17. The method of claim 14, wherein a difference between a beginning of a first superframe at the first rate and a beginning of a second superframe at the second rate is determined by an amount of time required to perform the step of decoding the frame of data.

18. The method of claim 14, further comprising the steps of:

providing a decoded frame of data to one of a first portion or a second portion of the rate adaptation buffer; and

moving the decoded frame of data to a third portion of the rate adaptation buffer from the first portion or the second portion before a new frame of data which follows the decoded frame of data by two frames.

* * * * *

STANDARDS PROJECT: Standards Project for Interfaces Relating to Carrier to Customer Connection of Asymmetric Digital Subscriber Line (ADSL) Equipment

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ABSTRACT: This document was prepared through a joint effort of the general editor and the associate editor, John Bingham (Amati Communications Corp.).

This WORKING DRAFT is provided for further study and review by the T1E1.4 Working Group. All of the proposed text introduced up to and including that provided at the October interim meeting has been merged into this document.

Editorial notes are provided throughout to indicate the current status of the proposed text and its source.

Secretariat

Exchange Carriers Standards Association

Abstract *(Preliminary Draft)*

This interface standard was written to provide the minimal set of requirements to provide for satisfactory transmission between the network and the customer installation. Equipment may be implemented with additional functions and procedures.

This standard presents the electrical characteristics of the Asymmetric Digital Subscriber Line (ADSL) signals appearing at the network interface. It also describes the physical interface between the network and the customer installation. The transport medium of the signals is a single twisted-wire pair that supports both Plain Old Telephone Service (POTS) and full-duplex (i.e., simultaneous two-way) and simplex (from the network to the customer installation) digital services.

Approved Month__, 19__

American National Standards Institute, Inc.

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PA = Provisionally Agreed, US= Under Study

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1 Scope, purpose and structure

**********EDITORIAL NOTE**********

Sub-clause 1.1
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1.1 Scope

This standard describes the interface between the telecommunications network and the customer installation in terms of the their interaction and electrical characteristics. The requirements of this standard apply to a single asymmetric digital subscriber line (ADSL). ADSL allows the provision of "plain old telephone service" (POTS) and a variety of possible digital channels. The digital channels may consist of a variety of possible low speed full-duplex channels and high speed simplex channels in the direction from network to customer premises. In this standard, the telecommunications network is referred to as the network, and the customer premises wiring and equipment, including the ATU-R and the POTS splitter, as the customer installation (CI). The interface between the network and the CI will be known as the network interface (NI).

The transmission system is designed to operate on two-wire twisted metallic cable pairs with mixed gauges. The standard is based on the use of cables without loading coils, but bridged taps are acceptable with the exception of unusual situations.

Specifically, the scope of this standard is as follows:

a) It describes the transmission technique used to support the simultaneous transport of POTS and both simplex and full-duplex digital channels on a single twisted-pair ;

b) It defines the combined options and ranges of digital simplex and full-duplex channels provided;

c) It specifies both the input signal with which the ATU-R must operate and the output signal the ATU-R must produce;

d) It defines the line code to be used, and spectral composition of the transmitted and received signals;

e) It describes the electrical and mechanical specifications of the network interface;

f) It describes the organization of transmitted and received data into frames;

g) It defines the functions of the operations channel ;

h) It defines the ATU-R to service module(s) interface functions.

1.2 Purpose TBP

1.3 Structure TBP

2. Normative referenced standards

2.1 Referenced American National Standards

This standard is intended for use in conjunction with the following American National Standards. When these referenced standards are superseded by a revision approved by the American National Standards Institute, Inc., the revision shall apply.

[1] ANSI T1.401-1992, Interface between carriers and customer installations analog voicegrade switched access lines using loop-start and ground-start signaling.

[2] ANSI/EIA/TIA - 571, Environmental considerations for telephone terminals, 1991

[3] dpANS T1.231-1993, In-service layer 1 digital transmission performance monitoring

3 Definitions, abbreviations, acronyms, and symbols

3.1 Definitions

3.1.1

3.2 Abbreviations, acronyms, and symbols

ac	alternating current
CI	customer installation
CO	central office
dB	decibels
dBm	decibels referred to 1 milliwatt
dc	direct current
Hz	hertz
NI	network interface
ms	millisecond
POTS	Plain old telephone service

4 Reference Models

**********EDITORIAL NOTE**********

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4.1 System reference model

The system reference model illustrates the various functional blocks required to provide ADSL service.

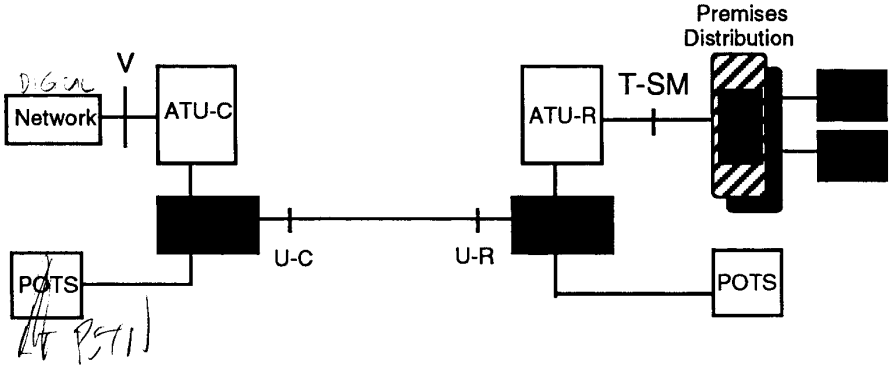

Figure 4.1 - ADSL Functional Reference Model

Definitions:

ATU-C: ADSL transmission unit at the CO end
ATU-R: ADSL transmission unit at the remote end
POTS: Plain old telephone service
Splitter: filter which separates high and low frequency signals at the CO end and remote end
SM: Service module, performs terminal adaption functions
T-SM: interface(s) between ATU-R and SM(s)
U-R: loop interface at remote (customer) end
U-C: loop interface at central office end
V: logical interface between ATU-C and network element such as one or more switching systems

Notes:

1. The V interface is defined in terms of logical functions; not physical.
2. The V interface may consist of interface(s) to one or more switches.
3. Implementation of the following interfaces are optional when interfacing elements are integrated into a common element: V, T-SM.
4. The splitter function may be integrated within the ATU
5. A digital carrier facility (e.g., SONET extension) may be interposed at the V interface when the ATU-C is located at a remote site.
6. The nature of the premises distribution (e.g., bus or star, type of media) are for further study.
7. More than one type of T-SM interface may be defined, and more than one type of T-SM interface might be provided from an ATU-R.
8. The ADSL eoc flows between the ATU-C and the ATU-R, extension of the eoc to the terminal equipment is for further study.

9. Due to the asymmetry of the signals on the line, the transmitted signals must be distinctly specified at the U-R and U-C reference points.

**********EDITORIAL NOTE**********

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5. Transport Capacity

An ADSL system may transport up to seven bearer channels simultaneously:

- up to four downstream simplex bearers (unidirectional from the network to the customer premises), and
- up to three duplex bearers (bi-directional between network and customer).

The net data rate transport capacity of an ADSL system will depend on the characteristics of the loop on which the system is deployed. *This section will not define loop classes, but rather, will define Transport Classes that differ in the net data rate, where net rates will be based on a set of default bearer channel rates. Definition of loop range classifications and recommendations for Transport Class(es) use on each loop classification may be provided in an informative Annex.*

Default data rates for the downstream simplex bearers are based on multiples of 1.536 Mbit/s up to 6.144 Mbit/s, leading to four possible transport classes. The ADSL data multiplexing format is designed to be flexible enough to allow other transport data rates, such as channelizations based on 1.544 or 2.048 Mbit/s structures.

Each bearer channel will be individually assigned to an ADSL sub-channel for transport. For the downstream simplex channels, i.e. those transported only from the server to the customer, the ADSL sub-channel rate will match the bearer rate, with the assignments described in Section 5.4; for the duplex channels, the ADSL sub-channel rates are fixed.

The aggregate data rate transmitted by an ADSL system will depend on the net data rate transported and on certain configurable options that affect overhead, such as allocation of user data streams to interleaving or non-interleaving data buffers within the ADSL frame (discussed in Sections 6.2, 6.4.2, 7.2, and 7.4.2).

Note 1: "Bearers" as used in this document has the meaning "bearer channels", which is a user data stream that carries a bearer service through an ADSL link. ADSL sub-channels (such as AS0, AS1, LS0, etc.) refer to ATU interface ports and to blocks of bytes within the ADSL framing structure.

Note 2: The default bearer channel rates are based on unframed 1.536 Mbit/s structures to be consistent with the expected evolution of network switching. Early ADSL deployments may need to interwork with DS1 (1.544 Mbit/s) data. The ADSL system overhead and data synchronization (see Section 6.2.2) provides enough capacity to support the framed DS1 data streams transparently (i.e., the entire DS1 signal is passed transparently through the ADSL transmission path without interpretation or removal of the framing bits and other DS1 overhead).

5.1 Simplex Bearers

Note: Simplex bearers in the downstream direction are specified herein; the use of upstream simplex bearer(s) is for further study.

5.1.1 Default Rates for Downstream Simplex Bearers

The default data rates for the four possible bearer channels that may be transported from the network to the customer premises (in the downstream direction, i.e., from ATU-C to ATU-R only) over an ADSL system are

- 1.536 Mbit/s
- 3.072 Mbit/s
- 4.608 Mbit/s

– 6.144 Mbit/s.

The ADSL system will use up to four sub-channels, named AS0, AS1, AS2, and AS3 to transport the downstream simplex bearer channels. An ADSL sub-channel's rate will match the rate of the bearer channel that it transports, subject to the following restrictions:

ADSL Sub-channel	AS0: n_0 x 1.536 Mbit/s,	n_0 = 0, 1, 2, 3 or 4;
	AS1: n_1 x 1.536 Mbit/s,	n_1 = 0, 1, 2, or 3;
	AS2: n_2 x 1.536 Mbit/s,	n_2 = 0, 1, or 2;
	AS3: n_3 x 1.536 Mbit/s,	n_3 = 0 or 1.

The maximum number of sub-channels that may be active at any given time and the maximum number of bearer channels that can be transported simultaneously by an ADSL system will depend on the transport class (as described in Sections 5.1.1.1 through 5.1.1.4 below) that can be supported by the specific loop and the configuration of the active sub-channels.

Note: An ADSL system could support switching on demand among the configurations allowed by the transport class that is supported. This subject is for further study.

5.1.1.1 Downstream Simplex Bearer Configurations for Default Transport Class 1 (Shortest Range, Highest Capacity)

The default simplex bearer capacity on Transport Class 1 is 6.144 Mbit/s, which may be composed of any combination of one to four bearer channels with n x 1.536 Mbit/s rates. Systems, at their option, may provide any and all bearer rates. Configuration options may include any subset of the following:

1) One 6.144 Mbit/s bearer channel,
2) One 4.608 Mbit/s bearer channel and one 1.536 Mbit/s bearer channel,
3) Two 3.072 Mbit/s bearer channels,
4) One 3.072 Mbit/s bearer channel and two 1.536 Mbit/s bearer channels, or
5) Four 1.536 Mbit/s bearer channels.

5.1.1.2 Downstream Simplex Bearer Configurations for Default Transport Class 2

The default simplex bearer capacity on Transport Class 2 is 4.608 Mbit/s, which may be composed of any combination of one to three bearer channels with n x 1.536 Mbit/s rates. Systems, at their option, may provide any and all bearer rates. Configuration options may include any subset of the following:

1) One 4.608 Mbit/s bearer channel,
2) One 3.072 Mbit/s bearer channel and one 1.536 Mbit/s bearer channel, or
3) Three 1.536 Mbit/s bearer channels.

5.1.1.3 Downstream Simplex Bearer Configurations for Default Transport Class 3

The default simplex bearer capacity on Transport Class 2 is 3.072 Mbit/s, which may be composed of one or two bearer channels with n x 1.536 Mbit/s rates. Systems, at their option, may provide either or both bearer rates. Configuration options may include any subset of the following:

1) One 3.072 Mbit/s bearer channel, or
2) Two 1.536 Mbit/s bearer channels.

5.1.1.4 Downstream Simplex Bearer Configurations for Default Transport Class 4 (Longest Range, Lowest Capacity)

Only one downstream simplex bearer option can be supported in Transport Class 4, and the default bearer channel capacity is

1) One 1.536 Mbit/s bearer channel.

5.1.2 Options for Providing 2.048 Mbit/s Downstream Simplex Bearers

ADSL equipment providers may include other channelization options in their product offerings. To ensure compatibility of the ADSL core modem with bearer channels based on 2.048 Mbit/s, data rates are treated in this section for the purposes of data multiplexing only (loop ranges, signals at the V- or T-interfaces, and compliance testing will not be addressed by this standard for these optional rates).

Bearer channels based on 2.048 Mbit/s that may optionally be transported from the network to the customer premises (in the downstream direction, i.e., from ATU-C to ATU-R only) over an ADSL system are

- 2.048 Mbit/s
- 4.096 Mbit/s
- 6.144 Mbit/s.

Note: The entire framed 2.048 Mbit/s structure is treated as a bearer data stream; the use of a lower payload rate is for further study.

An ADSL system supporting these options could use up to three of the Downstream Simplex sub-channels, AS0, AS1 and AS2, to transport the bearer channels. An ADSL sub-channel's rate will match the rate of the bearer channel that it transports, subject to the following restrictions:

ADSL Sub-channel	AS0:	n_0 x 2.048 Mbit/s,	n_0 = 0, 1, 2, or 3;
	AS1:	n_1 x 2.048 Mbit/s,	n_1 = 0, 1, or 2;
	AS2:	n_2 x 2.048 Mbit/s,	n_2 = 0 or 1.

The maximum number of sub-channels that may be active at any given time and the maximum number of bearer channels that can be transported simultaneously by an ADSL system will depend on the transport class (as described in Sections 5.1.2.1 through 5.1.2.3 below) that can be supported by the specific loop on which the system is deployed and the configuration of the active sub-channels.

5.1.2.1 Downstream Simplex Bearer Configurations for Optional Transport Class 2M-1

The simplex bearer capacity on the optional Transport Class 2M-1 is 6.144 Mbit/s, which may be composed of any combination of one to three bearer channels with n x 2.048 Mbit/s rates. Systems, at their option, may provide any and all bearer rates. Configuration options may include any subset of the following:

1) One 6.144 Mbit/s bearer channel,
2) One 4.096 Mbit/s bearer channel and one 2.048 Mbit/s bearer channel, or
3) Three 2.048 Mbit/s bearer channels.

5.1.2.2 Downstream Simplex Bearer Configurations for Optional Transport Class 2M-2

Combined simplex bearer capacity on the optional Transport Class 2M-2 is 4.096 Mbit/s, which may be composed of one or two bearer channels with n x 2.048 Mbit/s rates. Systems, at their option, may provide either or both bearer rates. Configuration options may include any subset of the following:

1) One 4.096 Mbit/s bearer channel, or
2) Two 2.048 Mbit/s bearer channels.

5.1.2.3 Downstream Simplex Bearer Configurations for Optional Transport Class 2M-3

Only one downstream simplex bearer option can be supported in the optional Transport Class 2M-3:

1) One 2.048 Mbit/s bearer channel.

5.1.3 Upstream Simplex Bearers.

For further study.

5.2 Duplex Bearers

Up to two or three duplex bearer channels may be transported simultaneously by an ADSL, depending on the loop characteristics and the rate of the second optional duplex bearer. The control channel (C) is mandatory; two other channels are optional: 160 kbit/s (which may be used to transport ISDN BRA) and 384 or 576 kbit/s. If the second optional channel carries a 384 kbit/s bearer, then the 160 kbit/s channel may also be transported by the ADSL; if the second optional channel carries 576 kbit/s, then the 160 kbit/s channel can not be transported.

Up to three bi-directional ADSL sub-channels may be active, depending on the loop characteristics and the options implemented. The C channel is transported either by ADSL sub-channel LS0 or entirely within the synchronization overhead available to the duplex channels. When the 160 kbit/s option is provided, the duplex bearer is transported by ADSL sub-channel LS1 . When the 384 or 576 kbit/s option is provided, it is transported by ADSL sub-channel LS2. Note that, depending on the maximum aggregate rate that can be supported on the specific loop and the options implemented, certain allowed combinations or none of the optional duplex ADSL sub-channels may be active in a given configuration (the control channel is always active).

5.2.1 Control Channel

The C channel will transport user-to-user (e.g., control of services) and user-to-network signaling (i.e., call setup and selection of services) for the downstream simplex bearer services and the 384 kbit/s or 576 kbit/s duplex service. It may also be used for the optional 160 kbit/s duplex bearer service when this service does not carry ISDN BRA (see Note). The C channel will operate at 16 kbit/s or 64 kbit/s in accordance with the Transport Class as follows:

Transport Class 4 or 2M-3 (maximum range loops):	16 kbit/s
All other Transport Classes:	64 kbit/s.

When operating at 16 kbit/s, the C channel is transported by the ADSL within the synchronization overhead (as defined in Section 6.2) dedicated to the duplex channels; when operating at 64 kbit/s, the C channel is transported by the ADSL sub-channel LS0.

Note: Signaling associated with the ISDN BRA (160 kbit/s) is carried by the D channel of the 2B + D signal embedded in the 160 kbit/s.

5.2.2 Optional Duplex Bearer Channels

Two optional duplex bearer channels may be transparently transported by an ADSL, depending on the loop characteristics. These optional bearers are
160 kbit/s, and
384 kbit/s or 576 kbit/s.

The default duplex options for the four transport classes are given in Table 5.2-1.

Note: The 160 kbit/s bearer would most likely carry ISDN BRA (160 kbit/s = 2B + D + overhead). An option to carry a 160 kbit/s clear channel is for further study.

Table 5.2-1. Default Maximum Optional Duplex Bearer Channels Supported by Transport Class

Transport Class	Optional Duplex Bearers that may be transported (Note 1)
1 or 2M-1 (minimum range)	Configuration 1: 160 kbit/s + 384 kbit/s Configuration 2: 576 kbit/s only
2, 3 or 2M-2 (mid range)	384 kbit/s only *(Note 2)*
4 or 2M-3 (maximum range)	160 kbit/s only

Note 1: When the 160 kbit/s optional duplex bearer is used to transport ISDN BRA, all signaling associated with the ISDN BRA (160 kbit/s) is carried by the D channel of the 2B + D signal embedded in the 160 kbit/s.

Signaling for the 576 kbit/s, 384 kbit/s and non-ISDN 160 kbit/s duplex bearers is included in the C channel, which is shared with the signaling for the downstream simplex bearer channels.

Note 2: Whether the defaults for Transport Classes 2, 3, or 2M-2 should support the 576 kbit/s optional duplex bearer is for further study.

5.3 ADSL System Overhead

ADSL system overhead includes:

-- capacity for synchronization of the simplex bearers,
-- capacity for synchronization of the duplex bearers,
-- synchronization control for the bearers transported with interleaving delay (interleave data buffer),
-- synchronization control for the bearers transported with no interleaving delay ("fast", or low-latency, data buffer),
-- an ADSL embedded operations channel, eoc,
-- an ADSL overhead control channel, aoc, (for on-line adaptation and reconfiguration, see Section 13),
-- crc check bytes, and
-- fixed indicator bits for OAM (Operations and Maintenance).

The bit rates set aside for various overhead functions is detailed in Section 5.5. For the downstream simplex bearer rates based on 1.536 Mbit/s, the maximum capacity available to eoc is approximately 29.7 kbit/s for Transport Classes 1, 2, and 3, and approximately 13.9 kbit/s for Transport Class 4. Actual eoc capacities will depend on the bearer channel rates and the data synchronization implementation.

Note: The eoc capacity is subject to change as overhead requirements evolve, or if other bearer rate options, such as transparent transport of 1.544 Mbit/s signals, are implemented.

5.4 Combined Options and Ranges

The maximum net downstream and upstream data rates (total bearer capacity) transported by an ADSL system depend on the loop characteristics and the bearer channel rates.

5.4.1 Options and Ranges for Default Bearer Channel Rates

For the default downstream simplex bearers, with rates based on 1.536 Mbit/s, up to four loop range options could be defined for ADSL transmission. This section does not treat default options for loop ranges, but rather for the transport classes discussed in Sections 5.1 and 5.2. *Definition of loop range classifications and recommendations for the transport class(es) that each loop range would support may be provided in an informative Annex.*

As shown in Sections 5.1 and 5.2, different ADSL sub-channel and bearer configuration options may be provided for each of the transport classes. The downstream simplex bearer configuration and the duplex bearer configuration may be treated independently. The net data rates (i.e., maximum bearer capacities) for the four possible transport classes based on the default bearer rates are summarized in Table 5.4-1. Systems, at their option, may provide any and all bearer rates.

Table 5.4-1. Bearer Channel Options by Transport Class for Default Bearer Rates (n x 1.536 Mbit/s)

Transport Class:	1	2	3	4
Downstream Simplex Bearers				
Maximum Capacity	6.144 Mbit/s	4.608 Mbit/s	3.072 Mbit/s	1.536 Mbit/s

Bearer Channel Options	1.536 Mbit/s, 3.072 Mbit/s, 4.608 Mbit/s, 6.144 Mbit/s	1.536 Mbit/s, 3.072 Mbit/s, 4.608 Mbit/s	1.536 Mbit/s, 3.072 Mbit/s	1.536 Mbit/s
Max. Active Subchannels	4 (AS0,AS1, AS2,AS3)	3 (AS0, AS1, AS2)	2 (AS0, AS1)	1 (AS0 only)
Duplex Bearers				
Maximum Capacity	640 kbit/s	448 kbit/s	448 kbit/s	176 kbit/s
Bearer Channel Options	576 kbit/s, 384 kbit/s, 160 kbit/s, C (64 kbit/s)	*(Note 1)* 384 kbit/s, C (64 kbit/s)	*(Note 1)* 384 kbit/s, C (64 kbit/s)	160 kbit/s, C (16 kbit/s)
Max. Active Subchannels	3 (LS0, LS1, LS2)	2 (LS0, LS2)	2 (LS0, LS2)	2 (LS0,LS1) (Note 2)

Note 1: Whether Transport Classes 2, 3, or 2M-2 should support the 576 kbit/s optional duplex bearer is for further study.

Note 2 : The 16 kbit/s "C" channel is carried entirely within the synchronization control overhead as described in Section 6.2, so that the LS0 sub-channel does not appear as a separate byte within the ADSL frame.

The possible configuration options for each transport class, showing assignment of bearer channels to ADSL sub-channels, are given in the following sections. The configuration is specified by the B_F and B_I parameters (described in Sections 6.2, 7.2, and 12.8) for each bearer channel.

5.4.1.1 Configuration Options for Default Transport Class 1

The default combined downstream simplex capacity for Transport Class 1 is 6.144 Mbit/s. Any subset of up to four ADSL sub-channels (AS0, AS1, AS2, and AS3) may be active. The higher rate bearer channels are restricted to lower-index ADSL sub-channels as shown in the simplex channel configurations in Table 5.4-2(a); systems, at their option, may provide any and all bearer rates, any subset of the ADSL sub-channels, and any subset of the configuration options in the table. The duplex bearer channel assignments are independent of the simplex assignments, and are shown in Table 5.4-2(b).

Table 5.4-2(a). Downstream Simplex Bearer Configuration Options with Allowable Assignment of Bearer Channels to ADSL Sub-Channels for Transport Class 1, Default Bearer Rates (1.536 Mbit/s)

	Bearer Channel Transported and ADSL Sub-Channel Rate (6.144 Mbit/s Total Capacity) (see Note)			
Configuration Option	Bearer Channels Transported	Sub-Channels on Which Bearer Channel may be transported	Number of Active Sub-Channels	Notes
1	1 -- 6.144 Mbit/s	AS0	1	AS1, AS2, AS3 not active
2	1 -- 4.608 Mbit/s 1 -- 1.536 Mbit/s	AS0 or AS1 AS0, AS1, AS2, AS3	2	two channels not active
3	2 -- 3.072 Mbit/s	AS0, AS1, or AS2	2	AS3 and one other channel not active
4	1 -- 3.072 Mbit/s 2 -- 1.536 Mbit/s	AS0, AS1, or AS2 AS0, AS1, AS2, AS3	3	one channel not active
5	4 -- 1.536 Mbit/s	AS0, AS1, AS2, AS3	4	all channels active

Note 1: "not active" means the sub-channel capability is implemented in the ADSL units, but cannot be active due to the maximum capacity and configuration constraints.

Note 2: A sub-channel is considered active if it is configured in the ADSL data multiplexing, and it may be transporting user data from end-to-end or carry an idle pattern.

Table 5.4-2(b). Duplex Bearer Configuration Options with Assignment of Bearer Channels to ADSL Sub-Channels for Transport Class 1, Default Bearer Rates

	Bearer Channel Transported and ADSL Sub-Channel Rate (Note 1)			
Configuration	Sub-Channel LS0	Sub-Channel LS1 (Note 2)	Sub-Channel LS2	Total Duplex Capacity
L0	C (64 kbit/s)	not active	576 kbit/s	640 kbit/s
L1	C (64 kbit/s)	160 kbit/s	384 kbit/s	608 kbit/s
L2	"	option n/a	384 kbit/s	448 kbit/s
L3	"	160 kbit/s	option n/a	224 kbit/s
L4	"	option n/a	option n/a	64 kbit/s

Note 1: "option n/a" denotes a case where the manufacturer chose not to include the optional duplex bearer channel.

Note 2: The 160 kbit/s option may be used to transport ISDN BRA (2B + D + overhead).

5.4.1.2 Configuration options for default transport class 2

For the default data rates, the maximum combined downstream simplex capacity for Transport Class 2 is 4.608 Mbit/s, and up to three ADSL sub-channels (AS0, AS1, and AS2) may be active. (The sub-channel AS3 is never used in these configuration options). The higher rate bearer channels are restricted to lower-index ADSL sub-channels as shown in the simplex channel configurations in Table 5.4-3(a); systems, at their option, may provide any and all bearer rates, any subset of the ADSL sub-channels, and any subset of the configuration options in the table. A 64 kbit/s control channel and an optional 384 kbit/s duplex channel are the defaults that can be supported by this transport class. The duplex bearer channel assignments are independent of the simplex assignments, and are shown in Table 5.4-3(b).

Table 5.4-3(a). Downstream Simplex Bearer Configuration Options with Assignment of Bearer Channels to ADSL Sub-Channels for Transport Class 2, Default Bearer Rates (1.536 Mbit/s)

	Bearer Channel Transported and ADSL Sub-Channel Rate (4.608 Mbit/s Total Capacity) (see Note)			
Configuration	Bearer Channels Transported	Sub-Channels on Which Bearer Channel may be transported	Number of Active Sub-Channels	Notes
1	1 -- 4.608 Mbit/s	AS0	1	AS1, AS2 not active
2	1 -- 3.072 Mbit/s 1 -- 1.536 Mbit/s	AS0 or AS1 AS0, AS1, AS2	2	one channel not active
3	3 -- 1.536 Mbit/s	AS0, AS1, AS2	3	all channels active

Note : "not active" means the sub-channel capability is implemented in the ADSL units, but cannot be active due to the maximum capacity and configuration constraints.

Table 5.4-3(b). Duplex Bearer Configuration Options with Assignment of Bearer Channels to ADSL Sub-Channels for Transport Class 2, Default Bearer Rates

	Bearer Channel Transported and ADSL Sub-Channel Rate (Notes 1,2)		
Configuration	Sub-Channel LS0	Sub-Channel LS2 (*Note 3*)	Total Duplex Capacity
L1	C (64 kbit/s)	384 kbit/s	448 kbit/s
L2	"	option n/a	64 kbit/s

Note 1: "option n/a" denotes a case where the manufacturer chose not to include the optional duplex bearer channel.

Note 2: The 160 kbit/s option is not supported and ADSL sub-channel LS1 is never used on this transport class.

Note 3: A configuration in which 576 kbit/s is allowed on sub-channel LS2 for this transport class is for further study.

5.4.1.3 Configuration options for default transport class 3

The default combined downstream simplex capacity for Transport Class 3 is 3.072 Mbit/s, and up to two ADSL sub-channels (AS0 and AS1) may be active. (The sub-channels AS2 and AS3 are never used in this transport class). The 3.072 Mbit/s bearer channel is restricted to ADSL sub-channel AS0 as shown in the simplex channel configurations in Table 5.4-4. Also shown in Table 5.4-4 are the possible duplex bearer channel assignments, which are the same as the duplex assignments allowed for Transport Class 2. Systems, at their option, may provide any and all bearer rates, any subset of the ADSL sub-channels, and any subset of the configuration options in the table.

Table 5.4-4. Bearer Channel Configuration Options with Assignment of Bearer Channels to ADSL Sub-Channels for Transport Class 3, Default Bearer Rates (1.536 Mbit/s)

	Bearer Channel Transported and ADSL Sub-Channel Rate				
	Downstream Simplex Sub-Channels (3.072 Mbit/s Total Capacity)		Duplex Sub-Channels (Note 1)		
Configuration	Sub-Channel AS0	Sub-Channel AS1 (Note 2)	Sub-Channel LS0	Sub-Channel LS2 (Notes 3,4)	Total Duplex Capacity
1	3.072 Mbit/s	(not active)	C (64 kbit/s)	384 kbit/s	448 kbit/s
2	"	"	"	option n/a	64 kbit/s
3	1.536 Mbit/s	1.536 Mbit/s	C (64 kbit/s)	384 kbit/s	448 kbit/s
4	"	"	"	option n/a	64 kbit/s

Note 1: LS1 sub-channel not supported or implemented for this transport class.
Note 2: "not active" means the sub-channel capability is implemented in the ADSL units, but cannot be active due to the maximum capacity and configuration constraints.
Note 3: "option n/a" denotes a case where the manufacturer chose not to include the optional duplex bearer channel.
Note 4: A configuration in which 576 kbit/s is allowed on sub-channel LS2 for this transport class is for further study.

5.4.1.4 Configuration options for default transport class 4

The default downstream simplex capacity for Transport Class 4 is 1.536 Mbit/s, and only the ADSL sub-channel AS0 may be active. Thus there is only one simplex configuration option. (The other three sub-channels not used in this transport class). Only a 16 kbit/s control channel and an optional 160 kbit/s duplex channel can be supported; the two possible configurations are shown in Table 5.4-5.

Table 5.4-5. Bearer Channel Configuration Options with Assignment of Bearer Channels to ADSL Sub-Channels for Transport Class 4, Default Bearer Rates (1.536 Mbit/s)

	Bearer Channel Transported and ADSL Sub-Channel Rate			
Configuration	Downstream Simplex Sub-Channel AS0	Duplex Sub-Channel LS0	Duplex Sub-Channel LS1 (Notes 1,2)	Total Duplex Capacity
1	1.536 Mbit/s	C (16 kbit/s)	160 kbit/s	176 kbit/s
2	"	"	option n/a	16 kbit/s

Note 1: The 160 kbit/s option may be used to transport ISDN BRA (2B + D + overhead).
Note 2: "option n/a" denotes a case where the manufacturer chose not to include the optional duplex bearer channel.

5.4.2 Options and ranges for bearer channel options based on 2.048 Mbit/s

For optional bearer rates based on 2.048 Mbit/s, up to three loop range options could be defined for ADSL transmission. This standards document will not address loop ranges for these optional bearer rates, but will provide configuration options for the three transport classes discussed in Sections 5.1 and 5.2

As shown in Sections 5.1 and 5.2, different ADSL sub-channel and bearer configuration options may be provided for each of the transport classes. The downstream simplex bearer configuration and the duplex bearer configuration may be treated independently. The maximum bearer capacities for the three possible transport classes for optional bearer

rates based on 2.048 Mbit/s are summarized in Table 5.4-6. Systems, at their option, may provide any and all bearer rates.

Table 5.4-6. Bearer channel options by transport class, optional bearer rates based on 2.048 Mbit/s

Transport Class:	2M-1	2M-2	2M-3
Downstream Simplex Bearers			
Maximum Capacity	6.144 Mbit/s	4.096 Mbit/s	2.048 Mbit/s
Bearer Channel Options	2.048 Mbit/s, 4.096 Mbit/s, 6.144 Mbit/s	2.048 Mbit/s, 4.096 Mbit/s	2.048 Mbit/s
Max. Active Subchannels	3 (AS0,AS1,AS2)	2 (AS0,AS1)	1 (AS0 only)
Duplex Bearers			
Maximum Capacity	640 kbit/s	448 kbit/s	176 kbit/s
Bearer Channel Options	576 kbit/s, 384 kbit/s, 160 kbit/s, C (64 kbit/s)	*(Note 1)* 384 kbit/s, C (64 kbit/s)	 160 kbit/s, C (16 kbit/s)
Max. Active Subchannels	3 (LS0, LS1, LS2)	2 (LS0, LS2)	2 (LS0, LS1) (Note 2)

Note 1: Whether Transport Class 2 should support the 576 kbit/s optional duplex bearer is for further study.

Note 2 : The 16 kbit/s "C" channel is carried entirely within the synchronization control overhead as described in Section 6.2, so that the LS0 sub-channel does not appear as a separate byte within the ADSL frame.

The possible configurations for each transport class, showing assignment of bearer channels to ADSL sub-channels, are given in the following sections. The configuration is specified by the B_F and B_I parameters (described in Sections 6.2, 7.2, and 12.8) for each bearer channel.

5.4.2.1 Configuration options for optional transport class 2M-1

The combined downstream simplex capacity for the optional Transport Class 2M-1 is 6.144 Mbit/s, and up to three ADSL sub-channels (AS0, AS1, and AS2) may be active. The higher rate bearer channels are restricted to lower-index ADSL sub-channels as shown in the simplex channel configurations in Table 5.4-7(a). Systems, at their option, may provide any and all bearer rates, any subset of the ADSL sub-channels, and any subset of the configuration options in the table. The duplex bearer channel assignments are independent of the simplex assignments, and are shown in Table 5.4-7(b).

Table 5.4-7(a). Bearer configuration options with assignment of bearer channels to ADSL sub-channels for optional transport class 2M-1 (minimum range), optional bearer rates based on 2.048 Mbit/s

	Bearer Channel Transported and ADSL Sub-Channel Rate (6.144 Mbit/s Total Capacity) (see Note)			
Configuration	Bearer Channels Transported	Sub-Channels on Which Bearer Channel may be transported	Number of Active Sub-Channels	Notes
1	1 -- 6.144 Mbit/s	AS0	1	AS1, AS2 not active
2	1 --4.608 Mbit/s 1 -- 2.048 Mbit/s	AS0 or AS1 AS0, AS1, AS2	2	one channel not active
3	3 -- 2.048 Mbit/s	AS0, AS1, AS2	3	all channels active

Note: "not active" means the sub-channel capability is implemented in the ADSL units, but cannot be active due to the maximum capacity and configuration constraints.

Table 5.4-7(b). Duplex bearer configuration options with assignment of bearer channels to ADSL sub-channels for optional transport class 2M-1 (minimum range)

	Bearer Channel Transported and ADSL Sub-Channel Rate (Note 1)			
Configuration	Sub-Channel LS0	Sub-Channel LS1 (Note 2)	Sub-Channel LS2	Total Duplex Capacity
L0	C (64 kbit/s)	not active	576 kbit/s	640 kbit/s
L1	C (64 kbit/s)	160 kbit/s	384 kbit/s	608 kbit/s
L2	"	option n/a	384 kbit/s	448 kbit/s
L3	"	160 kbit/s	option n/a	224 kbit/s
L4	"	option n/a	option n/a	64 kbit/s

Note 1: "option n/a" denotes a case where the manufacturer chose not to include the optional duplex bearer channel.

Note 2: The 160 kbit/s option may be used to transport ISDN BRA (2B + D + overhead).

5.4.2.2 Configuration options for optional transport class 2M-2

The combined downstream simplex capacity for the optional Transport Class 2M-3 is 4.608 Mbit/s, and up to two ADSL sub-channels (AS0 and AS1) may be active. (The sub-channel AS2 is never used in these configuration options). The 4.608 Mbit/s bearer channel is restricted to ADSL sub-channel AS0 as shown in the simplex channel configurations in Table 5.4-8. A 64 kbit/s control channel and an optional 384 kbit/s duplex channel can be supported on this transport class. The duplex bearer channel assignments are independent of the simplex assignments, and are also shown in Table 5.4-8. Systems, at their option, may provide any and all bearer rates, any subset of the ADSL sub-channels, and any subset of the configuration options in the table.

Table 5.4-8. Bearer configuration options with assignment of bearer channels to ADSL sub-channels for transport class 2 (mid range), optional bearer rates based on 2.048 Mbit/s

	Bearer channel transported and ADSL sub-channel rate				
	Downstream simplex sub-channels (4.096 Mbit/s Total Capacity)		Duplex sub-channels (Note 1)		
Configuration	Sub-Channel AS0	Sub-Channel AS1 (Note 2)	Sub-Channel LS0	Sub-Channel LS2 (Notes 3, 4)	Total Duplex Capacity
1	4.096 Mbit/s	(not active)	C (64 kbit/s)	384 kbit/s	448 kbit/s
2	"	"	"	option n/a	64 kbit/s
3	2.048 Mbit/s	2.048 Mbit/s	C (64 kbit/s)	384 kbit/s	448 kbit/s
4	"	"	"	option n/a	64 kbit/s

Note 1: LS1 sub-channel not implemented for this transport class.
Note 2: "not active" means the sub-channel capability is implemented in the ADSL units, but cannot be active due to the maximum capacity and configuration constraints.
Note 3: "option n/a" denotes a case where the manufacturer chose not to include the optional duplex bearer channel.
Note 4: Support of 576 kbit/s by Transport Class 2M-2 is for further study.

5.4.2.4 Configuration Options for Optional Transport Class 2M-3

The combined downstream simplex capacity for the optional Transport Class 2M-3 is 2.048 Mbit/s, and only the ADSL sub-channel AS0 may be active. Thus there is only one simplex configuration option. (ADSL sub-channels AS1 and AS2 are not used in these configuration options). Only a 16 kbit/s control channel and an optional 160 kbit/s duplex channel can be supported by Transport Class 2M-3; the two possible configurations are shown in Table 5.4-9.

Table 5.4-9. Bearer Configuration Options with Assignment of Bearer Channels to ADSL Sub-Channels for Transport Class 2M-3 (Maximum Range), Optional Bearer Rates based on 2.048 Mbit/s

	Bearer Channel Transported and ADSL Sub-Channel Rate			
Configuration	Downstream Simplex Sub-Channel AS0	Duplex Sub-Channel LS0 (Note 1)	Duplex Sub-Channel LS1 (Notes 2, 3)	Total Duplex Capacity
1	2.048 Mbit/s	C (16 kbit/s)	160 kbit/s	176 kbit/s
2	"	"	option n/a	16 kbit/s

Note 1: The 16 kbit/s "C" channel is carried entirely within the synchronization control overhead as described in Sections 6.2.2 and 7.2.2, so that the LS0 sub-channel does not appear at a fixed place within the ADSL frame.
Note 2: The 160 kbit/s option may be used to transport ISDN BRA (2B + D + overhead).
Note 3: "option n/a" denotes a case where the manufacturer chose not to include the optional duplex bearer channel.

5.5 Internal Overhead and Aggregate Bit Rates

The aggregate bit rate internally transmitted by the ADSL system includes capacity for the following:

1) the transported simplex bearer channels,
2) the transported duplex bearer channels, and
3) ADSL system overhead, which includes:
   -- capacity for synchronization of the simplex bearers (see Note),
   -- capacity for synchronization of the duplex bearers,
   -- synchronization control for the bearers transported with interleaving delay (interleave data buffer),
   -- synchronization control for the bearers transported with no interleaving delay ("fast", or low-latency, data buffer),
   -- an ADSL embedded operations channel, eoc,
   -- an ADSL overhead control channel (for on-line adaptation and reconfiguration (described in Section 13),
   -- crc check bytes, and
   -- fixed indicator bits for OAM (Operations and Maintenance).

Note: Synchronization control is described in Sections 6.2 and 7.2.

The organization of all the above data streams into ADSL frames and ADSL superframes is given in Section 6.2 for the data transmitted from ATU-C to ATU-R and in Section 7.2 for the data transmitted from ATU-R to ATU-C.

The internal overhead channels and their rates are shown in Table 5.5-1.

Table 5.5-1. Internal Overhead Channel Functions and Rates

	Maximum / Minimum / Typical Rate for Downstream (ATU-C to ATU-R)		Maximum / Minimum / Typical Rate for Upstream (ATU-R to ATU-C)	
	Transport Classes 1, 2, 3, 2M-1, or 2M-2 (Minimum and Mid Range Loops)	Transport Class 4 or 2M-3 (Maximum Range Loop)	Transport Classes 1, 2, 3, 2M-1, or 2M-2 (Minimum and Mid Range Loops)	Transport Class 4 or 2M-3 (Maximum Range Loop)
Synchronization capacity, shared among all bearers (Note 1)	128 / 64 / 96 kbit/s	96 / 64 / 96 kbit/s (Note 2)	64 / 32 / 64 kbit/s	64 / 32 / 64 kbit/s
Synchronization control and crc, interleave buffer	32 kbit/s	32 kbit/s	32 kbit/s	32 kbit/s
Synchronization control and crc, fast buffer, plus eoc and indicator bits	32 kbit/s	32 kbit/s	32 kbit/s	32 kbit/s
Total	192 / 128 / 160 kbit/s	160 / 128 / 160 kbit/s	128 / 96 / 128 kbit/s	128 / 96 / 128 kbit/s

Note 1: 64 kbit/s shared among simplex bearers within interleave buffer, 64 kbit/s shared among simplex bearers within fast buffer, an additional 0 or 32 kbit/s shared among duplex bearers within interleave buffer, and an additional 0 or 32 kbit/s shared among duplex bearers within fast buffer. Maximum rate occurs when at least one of each type of bearer is allocated to each type of buffer; minimum rate when all bearers are allocated to one buffer type. Typical rate allocates

bearers according to defaults described in Section 6.2 and assumes that all optional duplex bearers are implemented.

Note 2: Only one downstream simplex bearer available in Transport Class 4 or 2M-3 (Maximum Range Loops); the 64 kbit/s for synchronization of the simplex bearer to ADSL framing can appear in only one of the ADSL buffers (fast or interleaved).

The aggregate transmitted bit rate will depend on the transport class and implementation of optional duplex channels; components of the aggregate transmitted bit rate are summarized in Table 5.5-2 for downstream transmission and in Table 5.5-3 for upstream.

Table 5.5-2. Determination of Aggregate Bit Rate in the Downstream Direction (i.e., from ATU-C toward ATU-R)

	1.536 or 2.048 Mbit/s Bearers	Default Bearer channels (n x 1.536 Mbit/s)			Optional Bearers based on 2.048 Mbit/s (Note 1)	
	Transport Class 1	Transport Class 2 *(Note 2)*	Transport Class 3 *(Note 2)*	Transport Class 4	Transport Class 2M-2 *(Note 2)*	Transport Class 2M-3
Total downstream simplex bearer capacity	6.144 Mbit/s	4.608 Mbit/s	3.072 Mbit/s	1.536 Mbit/s	4.096 Mbit/s	2.048 Mbit/s
Duplex C channel	64 kbit/s	64 kbit/s	64 kbit/s	(Note 3)	64 kbit/s	(Note 3)
Total for Optional Duplex Bearers	0, 160, 384, 544 , or 576 kbit/s (Note 4)	0, 160, or 384 kbit/s	0, 160, or 384 kbit/s	0 or 160 kbit/s	0, 160, or 384 kbit/s	0 or 160 kbit/s
Total Bearer Channel Capacity	6.208-6.784 Mbit/s	4.672-5.056 Mbit/s	3.136-3.520 Mbit/s	1.536-1.696 Mbit/s (Note 5)	4.160-4.544 Mbit/s	2.048-2.208 Mbit/s (Note 5)
Overhead Range (from Table 5.5-1)	128 - 192 kbit/s	128 - 192 kbit/s	128 - 192 kbit/s	128 - 160 kbit/s	128 - 192 kbit/s	128 - 160 kbit/s
Aggregate Rate Range (Typical)	6.336-6.976 Mbit/s (6.912 Mbit/s)	4.800-5.248 Mbit/s (5.216 Mbit/s)	3.264-3.712 Mbit/s (3.680 Mbit/s)	1.664-1.856 Mbit/s (1.824 Mbit/s)	4.288-4.736 Mbit/s (4.704 Mbit/s)	2.176-2.368 Mbit/s (2.336 Mbit/s)

Note 1: The optional Transport Class 2M-1 for bearers based on 2.048 Mbit/s has the same combined rates as the default Transport Class 1.

Note 2: If it is determined that Transport Classes 2, 3, and 2M-2 can support the 576 kbit/s optional duplex bearer, then the maximum total bearer channel capacity and maximum aggregate rate will increase by 32 kbit/s for these classes.

Note 3 : For Transport Classes 4 and 2M-3, the duplex C channel is 16 kbit/s, which is transported entirely within the overhead dedicated to synchronization capacity.

Note 4: 544 kbit/s obtained when the two 160 kbit/s and 384 kbit/s optional duplex bearers are both included.

Note 5 : Duplex C channel not included in Total Bearer Channel Rates for Transport Classes 4 and 2M-3-- it's included in the Overhead.

Table 5.5-3. Determination of Aggregate Bit Rate in the Upstream Direction (i.e., from ATU-R to ATU-C)

	Transport Class 1 or 2M-1	Transport Classes 2, 3 or 2M-2 (see Note 1)	Transport Class 4 or 2M-3
Duplex C channel	64 kbit/s	64 kbit/s	(see Note 2)
Optional Duplex Bearers	0, 160, 384, 544, or 576 kbit/s (Note 3)	0, 160, or 384 kbit/s	0 or 160 kbit/s
Total Bearer Channel Capacity	64 - 640 kbit/s	64 - 448 kbit/s	0 - 160 kbit/s (Note 4)
Overhead Range (from Table 5.5-1)	96 - 128 kbit/s	96 - 128 kbit/s	96 - 128 kbit/s
Aggregate Rate Range (Typical)	160 - 768 kbit/s (768 kbit/s)	160 - 576 kbit/s (576 kbit/s)	96 - 288 kbit/s (288 kbit/s)

Note 1: If it is determined that Transport Classes 2, 3, and 2M-2 can support the 576 kbit/s optional duplex bearer, then the maximum total bearer channel capacity and maximum aggregate rate will increase by 32 kbit/s for these classes.

Note 2 : For Transport Classes 4 and 2M-3, the duplex C channel is 16 kbit/s, which is transported entirely within the overhead dedicated to synchronization capacity.

Note 3 : 544 kbit/s obtained when both optional duplex bearers are included.

Note 4 : Duplex C channel not included in Total Bearer Channel Rates for Transport Classes 4 and 2M-3--it's included in the Overhead.

6. ATU-C Functional Characteristics

**********EDITORIAL NOTE**********

Sub-clause 6.1 to 6.2
Status : Under Study (Oct./93 Interim Mtg.)
Cont. 93-188R1
Source: Amati
NOTE:

The following revised text is proposed for Sections 6.1 and 6.2 of the Draft Standard for DMT ADSL. Major changes in the R1 version include the following:

(a) changes in the data framing (including definition of synchronization control codes) to be consistent with contribution T1E1.4/93-119R2, "Revised Data Framing and Synchronization Conventions for DMT ADSL" (October 4, Alexandria, VA);
(b) addition of a data scrambler between the crc and FEC; and
(c) addition of an optional 576 kbit/s duplex data channel.

The following additional changes have been made for the November 1993 T1E1.4 meeting, and are indicated with revision marks:

(a) update of coding parameters in the first three rows of Table6.2-4 and in all three rows of Table 6.2-5;
(c) changes to the 3rd paragraph in Section 6.2.1.2.1;
(d) changes to 5th paragraph in Section 6.2.1.2.2; and
(e) change in nomenclature from "Loop Class" to "Transport Class" to be consistent with the latest proposed text for Section 5.

****

6.1 ATU-C input and output data interfaces

The functional data interfaces at the ATU-C are shown in Figure 6.1-1. Input interfaces for the high-speed downstream simplex bearer channels are designated AS0 through AS3; input/output interfaces for the duplex bearer channels are designated LS0 through LS2. There may also be a duplex interface for operations, maintenance and control of the ADSL system; this interface is for further study.

The data rates of the input and output data interfaces at the ATU-C for the default configurations are specified in this section. The exact number of physical interfaces and the physical and electrical characteristics of these interfaces appear in Sections 10 and 16.

The total net bearer capacity that can be transmitted in the downstream direction (ATU-C to ATU-R) corresponds to the transport class as described in Section 5.4; the mix of data rates at the downstream simplex input interfaces is limited to a combination whose net bit rate does not exceed the net downstream simplex bearer capacity for the given transport class. Similarly, the rate of the duplex bearer at the LS0 interface and the availability of the LS1 and LS2 options correspond to the transport class as discussed in Section 5.4.

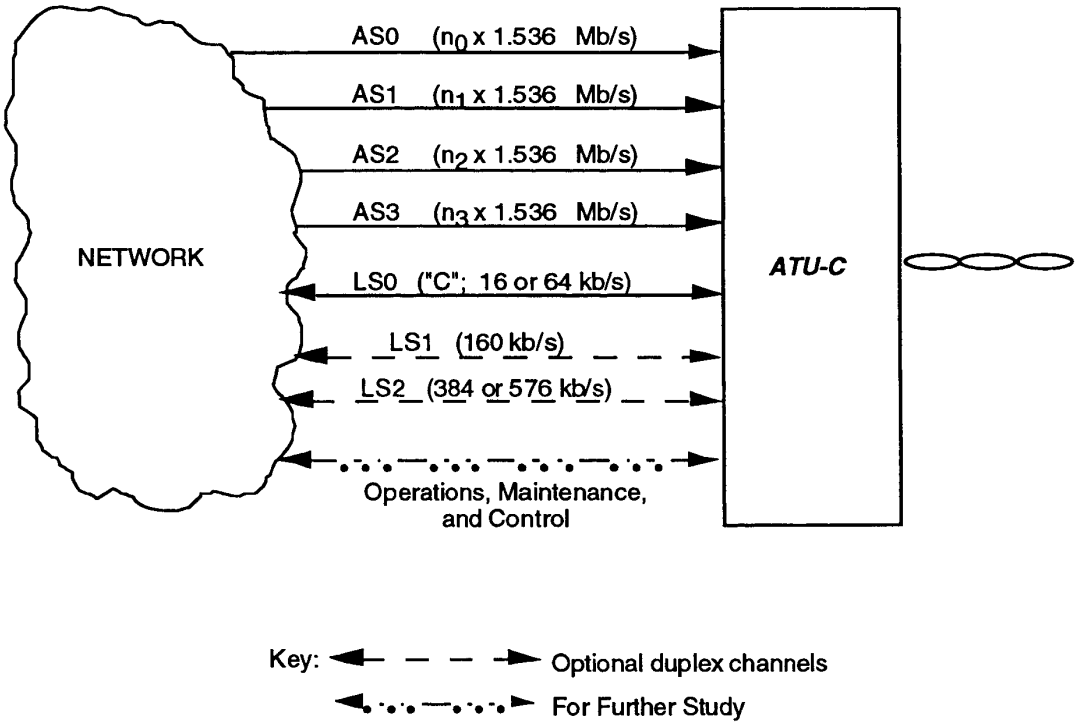


Figure 6.1-1. ATU-C Data Interfaces

6.1.1 Downstream simplex channels: transmit bit rates

The downstream simplex channels are transported in the downstream direction (ATU-C to ATU-R) only. The data interfaces at the ATU-C operate only as inputs.

6.1.1.1 Default Bearers based on 1.536 Mbit/s

There are four input interfaces at the ATU-C for the high-speed downstream simplex data channels: AS0, AS1, AS2 and AS3 (ASX in general). The data rates at these interfaces for the default configurations are n_X x 1.536 Mbit/s, where the allowed values of n_X are given in Table 6.1-1.

Table 6.1-1. Allowed data rates at the downstream simplex Input Interfaces to the ATU-C, for Default Configurations (n x 1.536 Mbit/s Bearers)

Downstream simplex Channel	Data Rates	Allowed Values of n_X
AS0	0, 1.536, 3.072, 4.608, or 6.144 Mbit/s	n_0 = 0, 1, 2, 3, or 4
AS1	0, 1.536, 3.072 or 4.608 Mbit/s	n_1 = 0, 1, 2 or 3
AS2	0, 1.536 or 3.072 Mbit/s	n_2 = 0, 1 or 2
AS3	0 or 1.536 Mbit/s	n_3 = 0 or 1

6.1.1.2 Option for bearers based on 2.048 Mbit/s

In an optional configuration for bearers based on 2.048 Mbit/s data streams, there are three input interfaces at the ATU-C for the high-speed downstream simplex data channels: AS0, AS1 and AS2 (ASX in general). (Input interface AS3 does not exist or is not connected internally). The data rates at these interfaces are n_x x 2.048 Mbit/s, where the allowed values of n_x are given in Table 6.1-2.

Table 6.1-2. Allowed Data Rates at the Downstream simplex Input Interfaces to the ATU-C, Optional Configuration (2.048 Mbit/s Bearers)

Downstream simplex Channel	Data Rates	Allowed Values of n_x
AS0	0, 2.048, 4.096, or 6.144 Mbit/s	n_0 = 0, 1, 2 or 3
AS1	0, 2.048, or 4.096 Mbit/s	n_1 = 0, 1 or 2
AS2	0 or 2.048 Mbit/s	n_2 = 0 or 1

6.1.2 Duplex Channels: Transmit and Receive Bit Rates

Both input and output data interfaces must be supplied at the ATU-C for the duplex bearers supported by the ADSL system.

Note: Two of the duplex channels are optional, as described in Section 5.2.2; the rate of the third duplex channel depends on the transport class, as defined in Section 5.2.1.

Table 6.1-3 shows the data rates that must be supported by both the input and output interfaces at the ATU-C for the duplex channels.

Table 6.1-3.
Interface data rates for duplex channels

Duplex Channel	Data Rate
LS0 (Note 1)	16 or 64 kbit/s
LS1 (Note 2)	160 kbit/s
LS2	384 kbit/s or 576 kbit/s
Operations, Maintenance, and Control (Note 3)	TBD

Note 1: LS0 is also known as the "C" or Control Channel. It carries the signaling associated with the ASX data streams and the 384 kbit/s or 576 kbit/s duplex data stream. When LS1 transports ISDN BRA, the signaling for LS1 is contained within the ISDN BRA D channel; if LS1 is used to transport a non-ISDN BRA data stream, then its signaling will also be contained in the "C" channel.

Note 2: LS1 may be used to carry Basic Rate ISDN (2B + D + overhead, where overhead includes all functions normally associated with the ISDN "U" Interface (ANSI T1.601)).

Note 3: This interface is for further study.

6.2 Framing

Framing of the downstream signal (ATU-C transmitter) is specified in this section. The upstream framing (ATU-R transmitter) is specified in Section 7.2.

6.2.1 Data Symbols

Figure 6.2-1 provides a functional block diagram of the ATU-C transmitter with reference points for data framing. Up to four downstream simplex data channels and up to three duplex data channels are multiplexed and synchronized

to the 4 kHz ADSL DMT symbol rate into two separate data buffers (fast and interleaved). A cyclic redundancy check (crc), scrambling, and forward error correction (FEC) coding are applied to each data buffer separately. The interleaved data buffer is then passed through an interleaving function. The fast and interleaved data buffers are then combined into a data symbol that is input to the Trellis Encoder. After Trellis Coding, the data is modulated to produce an analog signal for transmission across the customer loop.

No bit-level framing pattern is inserted in the data symbols of the frame or superframe structure. DMT symbol, or frame, boundaries are delineated by the cyclic prefix inserted by the modulator (see Section 6.9). Superframe boundaries are determined by the synchronization symbol which is also inserted by the modulator and which carries no user data (see Section 6.8).

Due to the addition of FEC parity bytes and due to data interleaving, the data symbols (i.e., bit-level data prior to Trellis Encoding) have different structural appearance at the different reference points through the transmitter. As shown in Figure 6.2-1, the reference points for which data framing will be described in the following subsections are

(A) "Mux data frame", the multiplexed, synchronized data after the crc is inserted (synchronization is described in Section 6.2.2, crc is specified in Section 6.2.1.3);
mux data frames will be generated at a nominal 4 kHz rate (i.e., each 250 msec);

(B) "FEC output data frame", the data frame generated at the output of the FEC encoder at the DMT symbol rate, where an FEC block may span more than one DMT symbol period; and

(C) "Trellis Encoder input data frame", the data frame presented to the Trellis Coder.

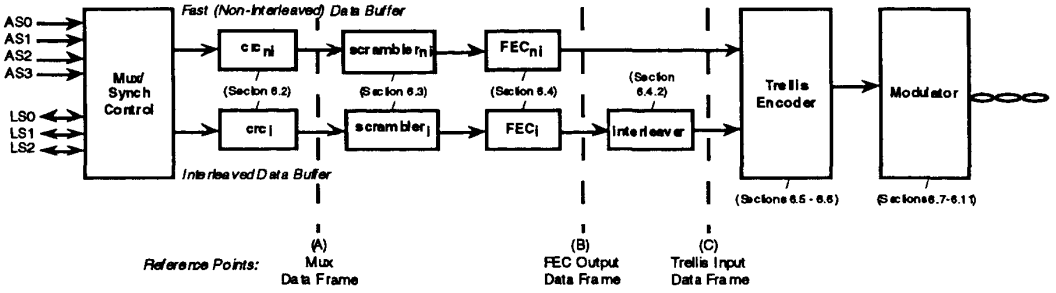


Figure 6.2-1. Reference Points for Data Framing, ATU-C Transmitter

6.2.1.1 Superframe Structure

ADSL uses the superframe structure shown in Figure 6.2-2. Each superframe is composed of 68 ADSL data frames, numbered from 0 to 67, which are encoded and modulated into multicarrier (DMT) symbols, followed by a synchronization symbol that is inserted by the modulator (see Section 6.7) to establish superframe boundaries. The synchronization symbol carries no user or overhead bit-level data; from the bit-level and user data perspective, DMT symbols have a nominal period of 250 msec (4000 frames/sec). (The modulator transmits an extra synch symbol after every 68 data symbols, so that the transmitted DMT symbol rate is 68/69 * 250 msec). Each data frame within the superframe contains a fast data buffer and an interleaved data buffer. The size of each buffer depends on the assignment of bearer channels made during initialization (see Section 6.2.1 and 12.8.4). (On-line reassignment of bearer channels is for further study).

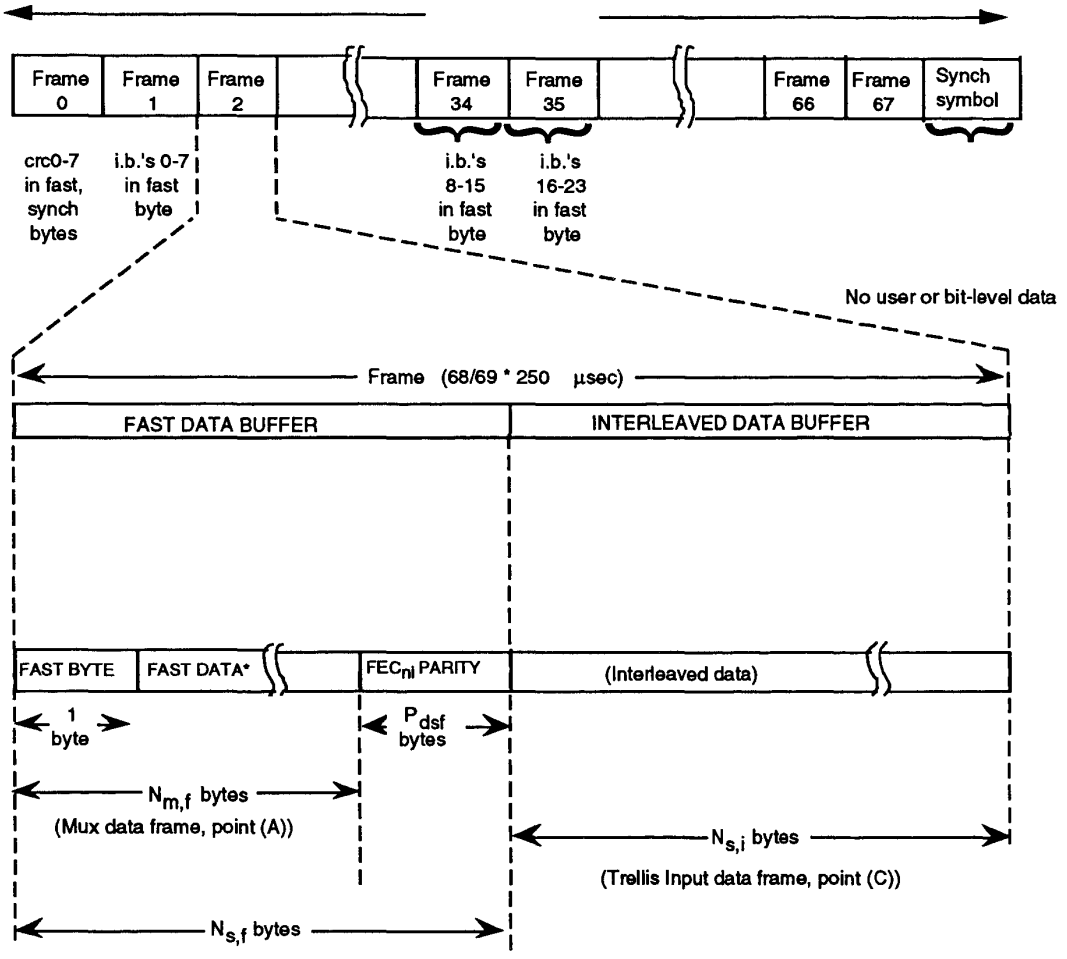


Figure 6.2-2. ADSL Superframe Structure, ATU-C Transmitter

Eight bits per ADSL superframe are reserved for the crc on the fast data buffer (crc0-crc7), and 24 indicator bits (ib0-ib23) are assigned for OAM functions. As shown in Figures 6.2-2 and 6.2-3, the "fast" byte of the fast data buffer carries the crc check bits in frame 0 and the fixed overhead bit assignments in frames 1, 34, and 35. The "fast" byte in other frames is assigned in even-/odd-frame pairs to either the eoc or to synchronization control of the bearer channels assigned to the fast buffer.

Note: Use of the "fast" byte to transport an OAM "EOC-like" data channel out to customer premises equipment is for further study (corresponds to certain functions at the interface labeled "Operations, Maintenance, and Control in Figure 6.1-1).

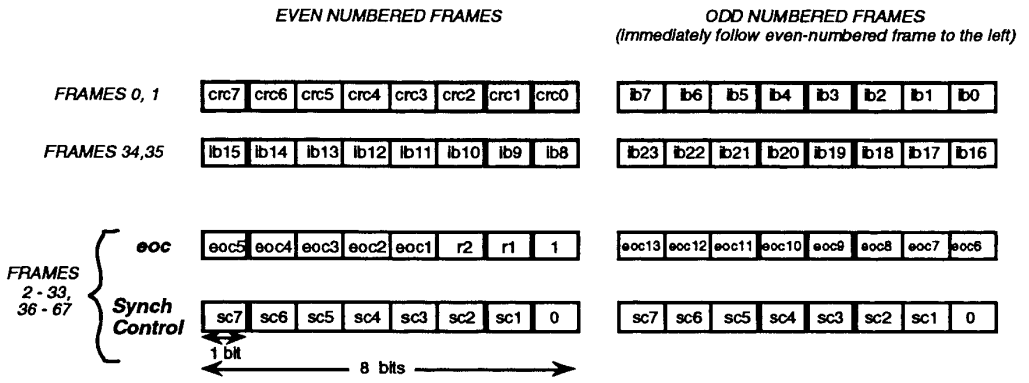


Figure 6.2-3. "FAST" Byte Format, ATU-C Transmitter, Fast Data Buffer

The indicator bits are defined in Table 6.2-1.

Table 6.2-1. Definition of indicator bits, ATU-C transmitter (Fast Data Buffer, Downstream direction)

Indicator Bit	Definition
ib0 - ib23	reserved for future use

If bit 0 of the "fast" byte in an even-numbered frame (other than frames 0 and 34) is "1", then the "fast" byte of that frame and the odd-numbered frame that immediately follows is used to carry a 13-bit "eoc frame", which is defined in Section 11.2 and in [1] as follows:

eoc1, eoc2	Address (11=ATU-C, 00=ATU-R, 01 and 10 reserved)
eoc3	Data/Mesage Indicator Bit: "0" = information field contains op code for ADSL eoc message, "1" = information field contains binary or ASCII data.
eoc4	Odd ("1") / Even ("0") byte indicator for multibyte transmission in data read or write mode
eoc5	Unspecified, set to 1 (reserved for future use) (see Note)
eoc6 - eoc13	Information field.

Note *Use of eoc5 to designate an autonomous message or an indicator message from the ATU-R that does not affect the eoc protocol state is for further study.*

The eoc protocol and message formats are described in Section 11.2 .

If bit 0 of the "fast" byte in an even-numbered frame (other than frames 0 and 34) is "0", then the "fast" byte of that frame and the odd-numbered frame that immediately follows is used for synchronization control (the "fast" byte format for synch control is described in Section 6.2.2.1).

Eight bits per ADSL superframe are reserved for the crc on the interleaved data buffer (crc_i0-crc_i7). As shown in Figures 6.2-2 and 6.2-4, the "synch" byte of the interleaved data buffer carries the crc check bits in frame 0. In all other frames (1 through 67), the "synch" byte is used for synchronization control of the bearer channels assigned to the interleaved data buffer or it is used to carry an ADSL overhead control channel (this latter use is for further study). When any bearer data streams appear in the interleave buffer, then the ADSL overhead control channel data is carried in the LEX byte, and the "synch" byte designates when the LEX byte contains this channel's data and when it contains data bytes from the bearer data streams. When no bearer data streams are allocated to the interleave data

buffer, i.e., all $B_F(ASX) = B_I(LSX) = 0$, then the "synch" byte carries the ADSL overhead control channel data directly (AEX and LEX do not exist in the interleave buffer in this case). The format of the "synch" byte is described in Section 6.2.2.2.

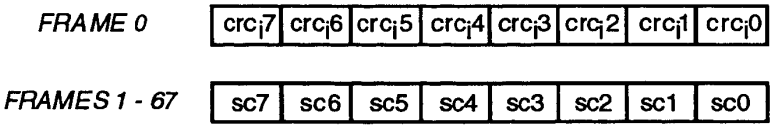


Figure 6.2-4. "Synch" Byte Format, ATU-C Transmitter, Interleaved Data Buffer

6.2.1.2 Frame structure

Each frame of data will be encoded into a multicarrier symbol, as described in Sections 6.3 through 6.6. As was shown in Figure 6.2-1, each frame is composed of a fast data buffer and an interleaved data buffer, and the frame structure has a different appearance at each of the reference points (A, B, and C). The bytes of the fast buffer will be clocked into the Trellis Encoder first, followed by the bytes of the interleaved data buffer. Bytes are clocked least significant bit first.

The assignment of user data streams to the fast and interleaved buffers is configured during initialization (see Section 11.6) with the exchange of a B_F, B_I pair for each data stream, where B_F designates the number of bytes of a given data stream to allocate to the fast buffer, and B_I designates the number of bytes allocated to the interleaved data buffer.

The possible values of B_F, B_I for a given data signal X are:

1) To place data signal X in the fast data buffer:
   $B_F(X) = 0$, $B_I(X)$ = Data Rate of X (bits/s) / 32000.
2) To place data signal X in the interleaved data buffer:
   $B_F(X)$ = Data Rate of X (bits/s) / 32000, $B_I(X) = 0$.

The seven possible B_F, B_I pairs are

$B_F(ASX)$, $B_I(ASX)$ for X = 0, 1, 2 and 3, for the downstream simplex channels, and
$B_F(LSX)$, $B_I(LSX)$ for X = 0, 1 and 2, for the duplex channels.

Default configurations (i.e., sets of B_F, B_I pairs) for the four possible transport classes is given in Table 6.2-2 for bearers based on 1.536 Mbit/s and in Table 6.2-3 for bearers based on 2.048 Mbit/s.

Note: On-line reconfiguration (e.g., changing the mix of downstream simplex data channel rates, reallocation of user data streams between fast and interleaved data buffers) is for further study.

Table 6.2-2. Default fast and interleaved data buffer allocations for ATU-C transmitter, Default Configurations (1.536 Mbit/s Bearers)

Signal	B_I (Interleaved Data Buffer) for Transport Classes 1 / 2 / 3 / 4	B_F (Fast Data Buffer) for Transport Classes 1 / 2 / 3 / 4
AS0	96 / 96 / 48 / 48	0 / 0 / 0 / 0
AS1	96 / 48 / 48 / 0	0 / 0 / 0 / 0
AS2	0 / 0 / 0 / 0	0 / 0 / 0 / 0
AS3	0 / 0 / 0 / 0	0 / 0 / 0 / 0
LS0	2 / 2 / 2 / 1 (Note 1)	0 / 0 / 0 / 0
LS1	0 / 0 / 0 / 0	5 / 0 / 0 / 5
LS2	0 / 0 / 0 / 0	12 / 12 / 12 / 0

Note 1 : In the case of Transport Class 4, $B_F(LS0) = 1$ or $B_I(LS0) = 1$ indicates a 16 kbit/s "C" channel, which is carried entirely within the synchronization control overhead as described in Section 6.2.2, so that the LS0 sub-channel does not appear as a separate byte within the ADSL frame.

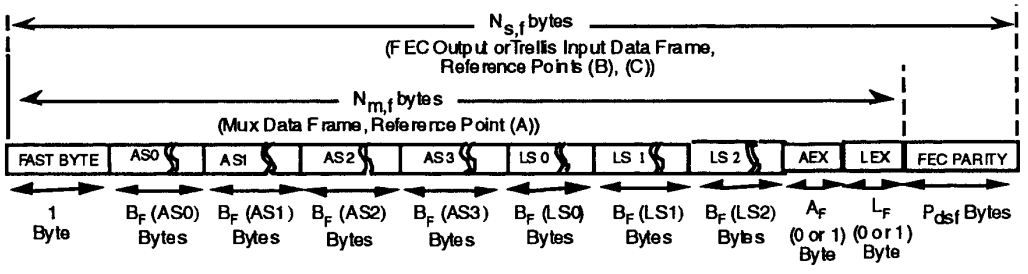
Table 6.2-3. Default fast and interleaved data buffer allocations for ATU-C transmitter, Optional Configuration (2.048 Mbit/s Bearers)

Signal	B_I (Interleaved Data Buffer) for Transport Classes 2M-1 / 2M-2 / 2M-3	B_F (Fast Data Buffer) for Transport Classes 2M-1 / 2M-2 / 2M-3
AS0	64 / 64 / 64	0 / 0 / 0
AS1	64 / 64 / 0	0 / 0 / 0
AS2	64 / 0 / 0	0 / 0 / 0
LS0	2 / 2 / 1 (Note 1)	0 / 0 / 0
LS1	0 / 0 / 0	5 / 0 / 5
LS2	0 / 0 / 0	12 / 12 / 0

Note 1: In the case of Transport Class 2M-3, $B_F(LS0) = 1$ or $B_I(LS0) = 1$ indicates a 16 kbit/s "C" channel, which is carried entirely within the synchronization control overhead as described in Section 6.2.2, so that the LS0 sub-channel does not appear as a separate byte within the ADSL frame.

6.2.1.2.1 Fast data buffer

The frame structure of the fast data buffer is shown in Figure 6.2-5 for the three reference points that were defined in Figure 6.2-1.



$$N_{m,f} = 1 + \sum_{i=0}^{3} B_F(AS_i) + A_F + \sum_{j=0}^{2} B_F(LS_j) + L_F,$$

where $A_F = \begin{cases} 0, & \sum_{i=0}^{3} B_F(AS_i) = 0, \\ 1 & \text{otherwise,} \end{cases}$

and

$$L_F = \begin{cases} 0, & \sum_{i=0}^{3} B_F(AS_i) = \sum_{j=0}^{2} B_F(LS_j) = 0, \\ 1 & \text{otherwise.} \end{cases}$$

$$N_{s,f} = N_{m,f} + P_{dsf},$$

where P_{dsf} = # FEC Parity Bytes.

Figure 6.2-5. Fast Data Buffer, ATU-C Transmitter

At reference point A, the Mux Data Frame, the fast buffer always contains at least the "fast" byte. This is followed by B_F(AS0) bytes of channel AS0, then B_F(AS1) bytes of channel AS1, B_F(AS2) bytes of channel AS2 and B_F(AS3) bytes of channel AS3. Next come the bytes for any duplex (LSX) channels allocated to the fast buffer. If any B_F(ASX) is non-zero, then both an AEX and an LEX byte follow the bytes of the last LSX channel, and if any B_F(LSX)is non-zero, the LEX byte must be included.

P_{dsf} FEC check bytes are added to the Mux data frame (reference point A) to produce the FEC output data frame (reference point B), where P_{dsf} is given in the RATES1 options used during Initialization. For the default configurations given in Tables 6.2-2 and 6.2-3, $P_{dsf} = 4$; for other configuration options, the value must be given to the ATU-C in some manner (for example, via a host control port). There always exists only one FEC codeword per symbol, so that the Trellis input data frame (reference point C) is identical to the FEC output data frame (reference point B).

6.2.1.2.2 Interleaved data buffer

The frame structure of the interleaved data buffer is shown in Figure 6.2-6 for the three reference points that were defined in Figure 6.2-1.

At reference point A, the Mux Data Frame, the interleaved data buffer always contains at least the "synch" byte. The rest of the buffer is built in the same manner as the fast buffer, substituting B_I in place of B_F. The length of each Mux data frame is $N_{m,i}$ bytes, where $N_{m,i}$ is defined in Figure 6.2-6.

The FEC coder will take in S Mux Data Frames and append P_{dsi} FEC parity bytes to produce the FEC codeword of length $N_{FEC,i} = S * N_{m,i} + P_{dsi}$. The FEC output data frames will contain $N_{s,i} = N_{FEC,i}/S$ bytes. When $S > 1$, then for the S frames in an FEC codeword, the FEC output Data Frame (reference point B) will partially overlap two Mux Data Frames for all but the last frame, which will contain the P_{dsi} FEC parity bytes.

The FEC output data frames are interleaved to a specified interleave depth. The interleaving process (see Section 6.4.2) delays each byte of a given FEC output data frame a different amount, so that the Trellis input data frames will contain bytes from many different FEC data frames. At reference point A in the transmitter, mux data frame 0 of the interleaved data buffer is aligned with the ADSL superframe and mux data frame 0 of the fast data buffer (this is not true at reference point C). At the receiver, the interleaved data buffer will be delayed approximately 16 msec with respect to the fast data buffer and frame 0 (containing the crc bits for the interleaved data buffer) will appear a fixed number of frames after the beginning of the receiver superframe (the exact delay will depend on the de-interleaver implementation, so is left to the vendor).

The FEC coding overhead, the number of symbols per FEC codeword, and the interleave depth are listed in Tables 6.2-4 and 6.2-5 for the default configurations (i.e, for all ASX signals plus LS0 allocated to the interleave buffer) that were given in Tables 6.2-2 and 6.2-3. These defaults correspond to the default data rates. For other rates and/or configurations, the coding parameters must be given to the ATU-C in some manner (for example, via a host control port).

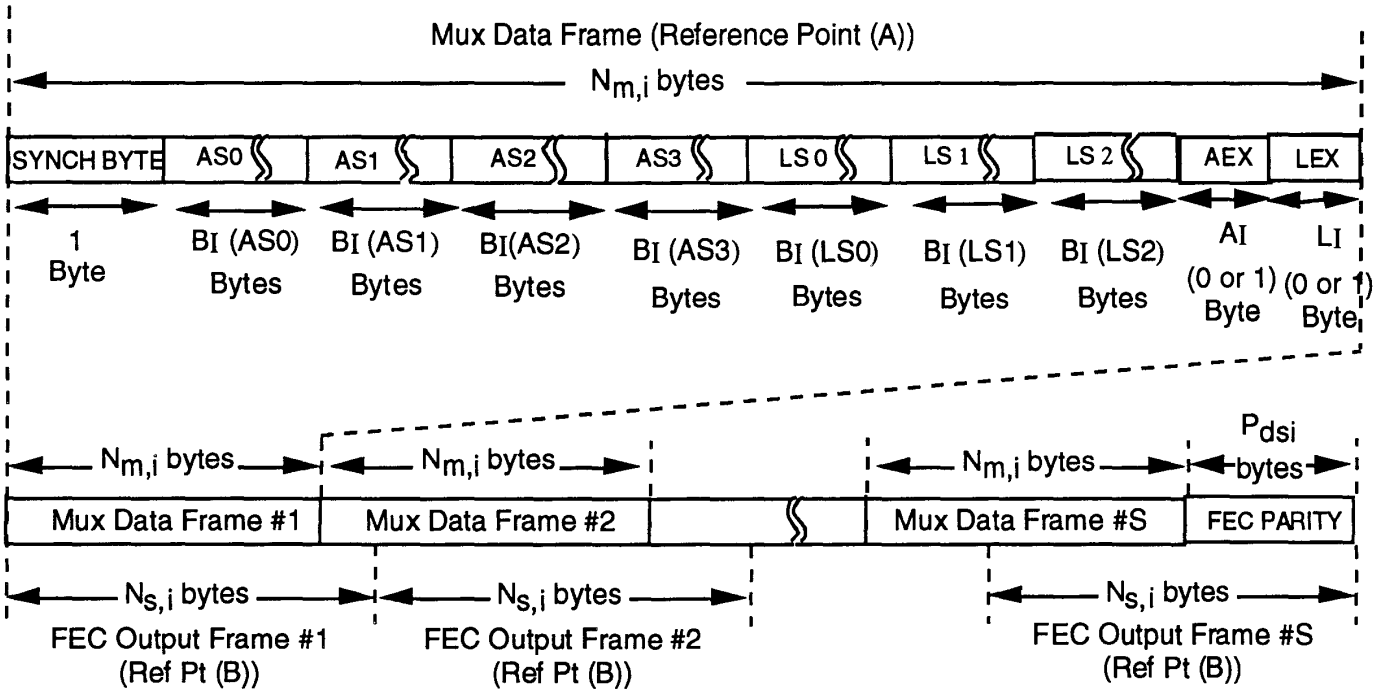
Table 6.2-4. Default FEC Coding Parameters and Interleave Depth, ATU-C Transmitter, Default Configurations (1.536 Mbit/s Bearers)

	P_{dsi} (FEC Parity Bytes)	S (symbols per codeword)	Interleave Depth (FEC codewords) (see Note)
Transport Class1	16	1	64
Transport Class 2	12	1	64
Transport Class 3	16	2	32
Transport Class 4	16	4	16
Synch Byte Only	4	4	16

Note: Interleave depths effect 16 msec latency for the interleave/deinterleave functions.

Table 6.2-5. Default FEC Coding Parameters and Interleave Depth, ATU-C Transmitter, Optional Configuration (2.048 Mbit/s Bearers)

Transport Class	P_{dsi} (FEC Parity Bytes)	S (symbols per codeword)	Interleave Depth (FEC codewords)
2M-1	16	1	64
2M-2	12	1	64
2M-3	12	2	32



$$N_{m,i} = 1 + \sum_{i=0}^{3} B_I(AS_i) + A_I + \sum_{j=0}^{2} B_I(LS_j) + L_I,$$

where $A_I = \begin{cases} 0, & \sum_{i=0}^{3} B_I(AS_i) = 0, \\ 1 & \text{otherwise,} \end{cases}$

and

$L_I = \begin{cases} 0, & \sum_{i=0}^{3} B_I(AS_i) = \sum_{j=0}^{2} B_I(LS_j) = 0, \\ 1 & \text{otherwise.} \end{cases}$

$$N_{s,i} = (S * N_{m,i} + P_{dsi}) / S,$$

where P_{dsi} = # FEC Parity Bytes,
and S = # DMT symbols per FEC codeword.

Figure 6.2-6: *Interleaved Data Buffer, ATU-C Transmitter*

6.2.1.3 Cyclic redundancy check (crc)

Two cyclic redundancy checks (crc's) are generated for each superframe: one for the fast data buffer and one for the interleaved data buffer. Eight bits per buffer type (fast or interleaved) per superframe are allocated to the crc function. The crc bits are

a) The "fast byte" (8 bits) of frame 0 in the fast data buffer, and
b) the "synch byte" (8 bits) of frame 0 in the interleaved data buffer.

The crc generating polynomial for both the fast data buffer and the interleaved data buffer is

$$D^8 + D^4 + D^3 + D^2 + 1,$$

where + denotes modulo 2 summation.

Each crc's shift register cells are set to 1 at the beginning of the superframe.
The bits covered by the crc include

1) For the fast data buffer:
   - Frame 0: ASX bytes (X = 0, 1, 2, 3),,LSX bytes (X = 0, 1, 2), followed by any AEX and LEX bytes.
   - All other frames: "fast" byte, followed by ASX bytes (X = 0, 1, 2, 3), LSX bytes (X = 0, 1, 2), and any AEX and LEX bytes.
2) For the interleaved data buffer:
   - Frame 0: ASX bytes (X = 0, 1, 2, 3), , LSX bytes (X = 0, 1, 2), . followed by any AEX and LEX bytes.
   - All other frames: "synch" byte, followed by ASX bytes (X = 0, 1, 2, 3), LSX bytes (X = 0, 1, 2), and any AEX and LEX bytes.

Each byte will be clocked into the crc least significant bit first.

Note that the crc field length will vary with the allocation of bytes to the fast and interleaved data buffers (the number of bytes in ASX and LSX vary according to the BF, BI pairs; AEX is present in a given buffer only if at least one ASX is allocated to that buffer; LEX is present in a given buffer only if at least one ASX or one LSX is allocated to that buffer).

[Note: Due to the flexibility in assignment of bearer channels to the fast and interleaved data buffers, crc field lengths over an ADSL superframe will vary from approximately 530 bits to approximately 116,000 bits; typical ranges will be TBD to TBD.]

6.2.2 Synchronization

The input data streams are synchronized to the ADSL clock using the synchronization control byte and the AEX and LEX bytes. Forward-error-correction coding is always applied to the synchronization control byte(s).

6.2.2.1 Synchronization for the fast data buffer

Synchronization control for the fast data buffer can occur in frames 2 through 33 and 36 through 67 of an ADSL superframe as described in Section 6.2.1.1, where the "fast" byte may be used as the synchronization control byte.

The format of the "fast" byte when used as synchronization control for the fast data buffer is *given in the following table:*

sc7, sc6	ASX channel designator	"00" : channel AS0 "01" : channel AS1 "10" : channel AS2 "00" : channel AS3
sc5, sc4	Synchronization control for the designated ASX channel	"00" : do nothing "01" : add AEX byte to designated ASX channel "11" : add AEX and LEX bytes to ASX channel "10" : delete last byte from designated ASX channel
sc3, sc2	LSX channel designator	"00" : channel LS0 "01" : channel LS1 "10" : channel LS2 "11" : do nothing to any LSX channel
sc1	Synchronization control for the designated LSX channel	"1" : add LEX byte to designated LSX channel "0" : delete last byte from designated LSX channel
sc0	Synch/eoc designator	"0" : perform synchronization control as indicated in sc7-sc1 "1" : this byte of current (even-numbered) frame and of frame that immediately follows is an eoc frame

No synchronization action is to be taken for frames in which the "fast" byte is used for crc, fixed indicator bits or eoc.

Note: Early ADSL deployments may need to interwork with DS1 (1.544 Mbit/s) or DS1C (3.142 Mbit/s) rates. The synchronization control option that allows adding up to two bytes to an ASX bearer channel provides sufficient overhead capacity to transport combinations of DS1 or DS1C channels transparently (without interpreting or stripping and regenerating the framing embedded within the DS1 or DS1C). The synchronization control algorithm must however guarantee that the fast byte in some minimum number of frames be available to carry eoc frames, so that a minimum (TBD) eoc rate may be maintained.

6.2.2.2 Synchronization for the interleaved data buffer

Synchronization control for the interleaved data buffer can occur in frames 2 through 67 of an ADSL superframe as described in Section 6.2.1.1, where the "synch" byte may be used as the synchronization control byte.

The format of the "synch" byte when used as synchronization control for the interleaved data buffer is *given in the following table:*

sc7, sc6	ASX channel designator	"00" : channel AS0 "01" : channel AS1 "10" : channel AS2 "00" : channel AS3
sc5, sc4	Synchronization control for the designated ASX channel	"00" : do nothing "01" : add AEX byte to designated ASX channel "11" : add AEX and LEX bytes to ASX channel "10" : delete last byte from designated ASX channel
sc3, sc2	LSX channel designator	"00" : channel LS0 "01" : channel LS1 "10" : channel LS2 "11" : do nothing to any LSX channel
sc1	Synchronization control for the designated LSX channel	"1" : add LEX byte to designated LSX channel "0" : delete last byte from designated LSX channel
sc0	Synch/aoc designator	"0" : perform synchronization control as indicated in sc7-sc1 "1" : LEX byte carries ADSL overhead control channel data

No synchronization action is to be taken during frame 0, where the "synch" byte is used for crc.

Note: Early ADSL deployments may need to interwork with DS1 (1.544 Mbit/s) or DS1C (3.142 Mbit/s) rates. The synchronization control option that allows adding up to two bytes to an ASX bearer channel provides sufficient overhead capacity to transport combinations of DS1 or DS1C channels transparently (without interpreting or stripping and regenerating the framing embedded within the DS1 or DS1C).

**********EDITORIAL NOTE**********

Sub-clause 6.3 to 6.6
Status : Under Study (Oct./93 Interim Mtg.)
Cont. 93-189R1
Source: Amati

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6.3 Scramblers

The binary data streams output from the fast and interleaved buffers are scrambled separately using the following algorithm for both:

$$d_n' = d_n + d_{n-18}' + d_{n-23}'$$

where + indicates modulo-two addition, d_n is the n-th output from the fast or interleaved buffer, and d_n' is the corresponding n-th output from either of the scramblers.

6.4 Forward error correction

6.4.1 Reed-Solomon coding

R redundant check bytes C_{R-1} , C_{R-2} , ... , C_1 , C_0 are appended to K message bytes M_{K-1} , M_{K-2} , ... , M_1 , M_0 to form a Reed-Solomon code word of size N = K + R bytes. The check bytes are computed from the message byte using the equation:

$C(z) = M(z)\, z^R$ modulo $G(z)$

where $C(z) = C_{R-1}\, z^{R-1} + C_{R-2}\, z^{R-2} + ... + C_1\, z + C_0$ is the check polynomial,

$M(z) = M_{K-1}\, z^{K-1} + M_{K-2}\, z^{K-2} + ... + M_1\, z + M_0$ is the message polynomial,

and $G(z) = \prod (z + \alpha^i)$ is the generator polynomial of the Reed-Solomon code, where the index of the product runs from i = 0 to R-1. In other words, C(z) is the remainder obtained from dividing $M(z)\, z^R$ by G(z). The arithmetic is performed in the Galois Field GF(2^8), where α is a primitive element that satisfies the primitive binary polynomial $x^8 + x^4 + x^3 + x^2 + 1$. A data byte (d_7 , d_6 , ... , d_1 , d_0) is identified with the Galois Field element

$d_7 \alpha^7 + d_6 \alpha^6 + ... + d_1 \alpha + d_0$

The number of check bytes R, and the codeword size N vary, as explained in Section 6.2.

6.4.2 Interleaving

The Reed-Solomon codewords in the interleave buffer are convolutionally interleaved. The interleaving depth D varies, as explained in the earlier section on framing, but it is always a power of 2. Convolutional interleaving is defined by the rule:

> Each of the N bytes X_0 , X_1 , ... , X_{N-1} in a Reed-Solomon codeword is delayed by an amount which varies linearly with the byte index. More precisely byte X_i (with index i) is delayed by (D-1) * i bytes, where D is the interleave depth.

An example for N = 5, D = 2 is shown in the following table where X^j_i denotes the i-th byte of the j-th codeword.

Inter-leaver Input	X^j_0	X^j_1	X^j_2	X^j_3	X^j_4	X^{j+1}_0	X^{j+1}_1	X^{j+1}_2	X^{j+1}_3	X^{j+1}_4
Inter-leaver Output	X^j_0	X^{j-1}_3	X^j_1	X^{j-1}_4	X^j_2	X^{j+1}_0	X^j_3	X^{j+1}_1	X^j_4	X^{j+1}_2

Table 6.4-1: Convolutional interleaving example for N = 5, D =2

With the above mentioned rule, and the chosen interleaving depths (powers of 2), the output bytes from the interleaver always occupy distinct time slots as long as N is odd. When N is even, a dummy byte is added at the beginning of the codeword at the input to the interleaver. The resultant odd-length codeword is then convolutionally interleaved, and the dummy byte then removed from the output of the interleaver.

6.5 Tone ordering

A DMT time-domain signal has a high peak-to-average ratio (its amplitude distribution is almost Gaussian), and large values may be clipped by the digital-to-analog converter. The error signal caused by clipping can be considered an additive negative impulse for the time sample that was clipped. The clipping error power is equally distributed across all tones in the symbol in which clipping occurs. It therefore is most likely to cause errors on those tones that, in anticipation of a higher received SNR, have been assigned the largest number of bits (and therefore have the densest constellations). These occasional errors can be reliably corrected by the FEC coding if the tones with the largest number of bits have been assigned to the interleave buffer.

The numbers of bits and the relative gains to be used for every tone are calculated in the ATU-R receiver, and sent back to the ATU-C according to a defined protocol (see later section). The pairs of numbers are typically stored, in ascending order of frequency or tone number i, in a Bit and Gain table.

The "tone-ordered" encoding assigns the first B_F bytes ($8B_F$ bits) from the symbol buffer (see earlier section on framing) to the tones with the smallest number of bits assigned to them, and the remaining B_I bytes ($8B_I$ bits) to the remaining tones.

The ordered bit table b'_i is based on the original bit table b_i as follows:

For k = 0 to 15 { From the bit table, find the set of all i with the number of bits per tone $b_i = k$
Assign b_i to the ordered bit allocation table in ascending order of i }

A complementary de-ordering procedure must be performed in the ATU-R receiver. It is not necessary, however, to send the results of the ordering process to the receiver because the bit table was originally generated in the ATU-R, which therefore has all information necessary to perform the de-ordering.

6.6 Encoder (trellis code version)

Block processing of Wei's 16-state 4-dimensional trellis code may be included to improve system performance. An algorithmic constellation encoder is used to construct constellations with a maximum of 15 bits.

6.6.1 Bit extraction

Data bytes from the DMT symbol buffer are extracted according to a re-ordered bit allocation table b'_i, using the least-significant-bit-first convention. Due to the 4-dimensional nature of the recommended code, the extraction is based on pairs of consecutive b'_i, rather than on individual ones, as in the non-trellis-coded case. Furthermore, due to the constellation expansion associated with trellis coding, the bit allocation table b'_i specifies the number of coded bits per tone. The bit allocation algorithm during initialization iterates directly on the number of coded bits per tone. The number of bits per tone b'_i can take any non-negative integer values not exceeding 15, with the exception of $b'_i = 1$. Given a pair (x,y) of consecutive b'_i, x+y-1 bits (reflecting a constellation expansion of 1 bit per 4 dimensions, or half bit per tone) are extracted from the DMT symbol buffer. These z = x+y-1 bits (t_z , t_{z-1} , .., t_1) are used to form the binary word u as shown in Table 6.6-1. The tone ordering procedure ensures $x \leq y$. Single-bit constellations are not allowed because they can be replaced by 2-bit constellations with the same average energy. Please refer to section 6.6.2 for the reason behind the special form of the word u for the case $x = 0$, $y > 1$.

Condition	Binary Word / Comment
$x > 1 , y > 1$	$u = (t_z , t_{z-1} , \ldots , t_1)$
$x = 1 , y \geq 1$	Condition not allowed
$x = 0 , y > 1$	$u = (t_z , t_{z-1} , \ldots , t_2 , 0 , t_1 , 0)$
$x = 0 , y \leq 1$	Bit extraction not necessary, no message bits being sent

Table 6.6-1: Forming the Binary Word u

The final two 4-dimensional symbols in the DMT symbol are chosen to force the trellis state to the zero state. For each of these symbols, the 2 lsbs of u are pre-determinded, and only x+y-3 bits are extracted from the DMT symbol buffer.

6.6.2 Bit conversion

The binary word $u = (u_{z'} , u_{z'-1} , \ldots , u_1)$ determines two binary words $v = (v_{z'-y} ,\ldots,v_0)$ and $w = (w_{y-1},\ldots,w_0)$, which are used to look up two constellation points in the encoder constellation table. For the usual case of x>1 and y>1, $z' = z = x+y-1$. Thus in this case v and w contain x and y bits respectively. For the special case of $x = 0$, $z' = z+2 = y-1$. In the latter case, $v = (v_1,v_0) = 0$ while $w = (w_1,w_0)$. The bits (u_3,u_2,u_1) determine (v_1 , v_0) and (w_1 , w_0) according to Figure 6.6-1 where the sign + denotes modulo-2 addition (exclusive-or)

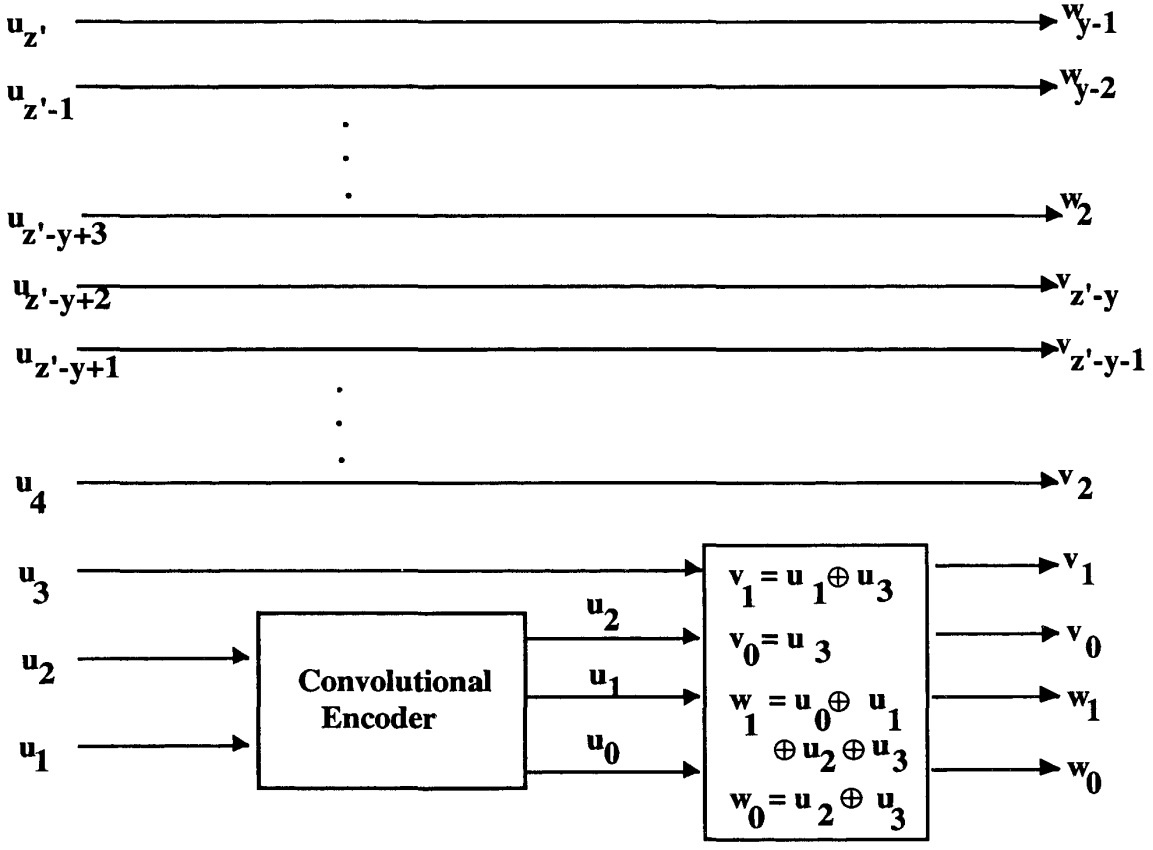

Figure 6.6-1: Conversion of u to v and w

The convolutional encoder shown in Figure 6.6-1 is a systematic encoder (i.e. u_1 and u_2 are passed through unchanged) as depicted in Figure 6.6-2. The states (S_3 , S_2 , S_1 , S_0) are used to label the states of the trellis diagram shown in Figure 6.6-4. The initial state (S_3 , S_2 , S_1 , S_0) is the zero state (0, 0, 0, 0) at the beginning of a DMT symbol period.

The remaining bits of v and w are obtained from the less significant and more significant parts of $(u_{z'}, u_{z'-1}, .. ,u_4)$, respectively. When x>1, y>1, $v = (u_{z'-y+2} , u_{z'-y+1} , ... , u_4, v_1, v_0)$ and $w = (u_{z'}, u_{z'-1} , ... ,u_{z'-y+3}, w_1, w_0)$. When x = 0, the bit extraction and conversion algorithms have been judiciously designed so that $v_1 = v_0 = 0$.

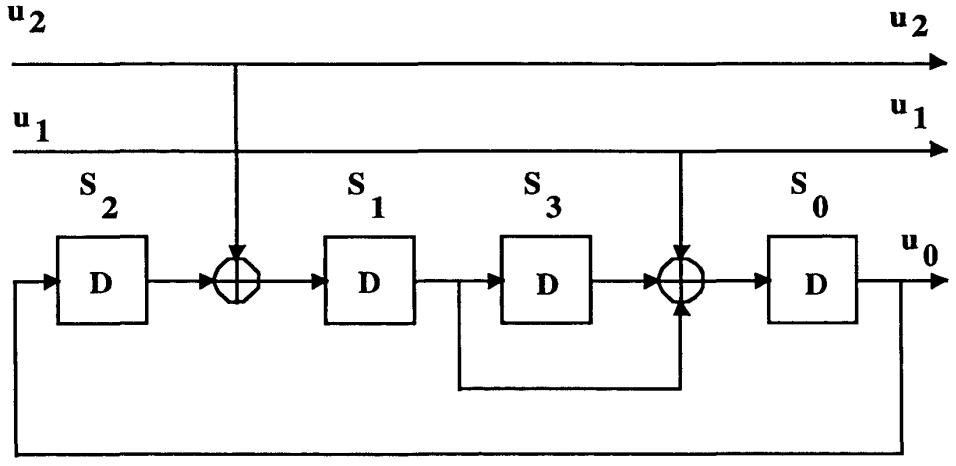

Figure 6.6-2: Finite state machine for Wei's encoder

In order to force the final state to the zero state (0,0,0,0), the 2 lsbs u_1 and u_2 of the final two 4-dimensional symbol in the DMT symbol are constrained to $u_1 = S_1 + S_3$, and $u_2 = S_2$, where + denotes exclusive-or.

6.6.3 Coset partition and trellis diagram

In a TCM system, the expanded constellation is labeled and partitioned into subsets using a technique called mapping by set-partitioning. These subsets are also called cosets. The four-dimensional cosets in Wei's code can each be written as the union of two Cartesian products of two 2-dimensional cosets. For example, $C_4^0 = (C_2^0 x C_2^0) U (C_2^3 x C_2^3)$. The four constituent 2-dimensional cosets, denoted by C_2^0 , C_2^1 , C_2^2 , C_2^3 , shown in Figure 6.6-3.

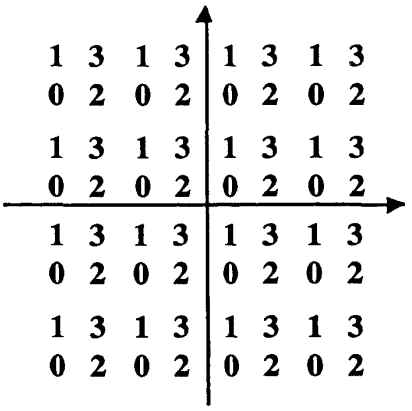

Figure 6.6-3: Constituent 2-dimensional cosets for Wei's code

The encoding algorithm guarantees that the 2 LSBs of a constellation point equals the index i of the 2-dimensional coset C_2^i in which the constellation point lies. The bits (v_1 , v_0) and (w_1 , w_0) are in fact the binary representations of these indices.

The three bits (u_2 , u_1 , u_0) are used to select one of the 8 possible four-dimensional cosets. The 8 cosets are labeled C_4^i where i is the integer with binary representation (u_2,u_1,u_0). The additional bit u_3 (see Figure 6.6-1) determines which of the two Cartesian products of 2-dimensional cosets in the 4-dimensional coset is chosen. The relationship is shown in Table 6.6-2. The bits (v_1,v_0) and (w_1,w_0) are computed from (u_3 , u_2 , u_1 , u_0) using the linear equations given in Figure 6.6-1.

4-D Coset	u_3 u_2 u_1 u_0	v_1 v_0	w_1 w_0	2-D Cosets
C_4^0	0 0 0 0 1 0 0 0	0 0 1 1	0 0 1 1	$C_2^0 \times C_2^0$ $C_2^3 \times C_2^3$
C_4^4	0 1 0 0 1 1 0 0	0 0 1 1	1 1 0 0	$C_2^0 \times C_2^3$ $C_2^3 \times C_2^0$
C_4^2	0 0 1 0 1 0 1 0	1 0 0 1	1 0 0 1	$C_2^2 \times C_2^2$ $C_2^1 \times C_2^1$
C_4^6	0 1 1 0 1 1 1 0	1 0 0 1	0 1 1 0	$C_2^2 \times C_2^1$ $C_2^1 \times C_2^2$
C_4^1	0 0 0 1 1 0 0 1	0 0 1 1	1 0 0 1	$C_2^0 \times C_2^2$ $C_2^3 \times C_2^1$
C_4^5	0 1 0 1 1 1 0 1	0 0 1 1	0 1 1 0	$C_2^0 \times C_2^1$ $C_2^3 \times C_2^2$
C_4^3	0 0 1 1 1 0 1 1	1 0 0 1	0 0 1 1	$C_2^2 \times C_2^0$ $C_2^1 \times C_2^3$
C_4^7	0 1 1 1 1 1 1 1	1 0 0 1	1 1 0 0	$C_2^2 \times C_2^3$ $C_2^1 \times C_2^0$

Table 6.6-2: Relation between 4-dimensional and 2-dimensional cosets

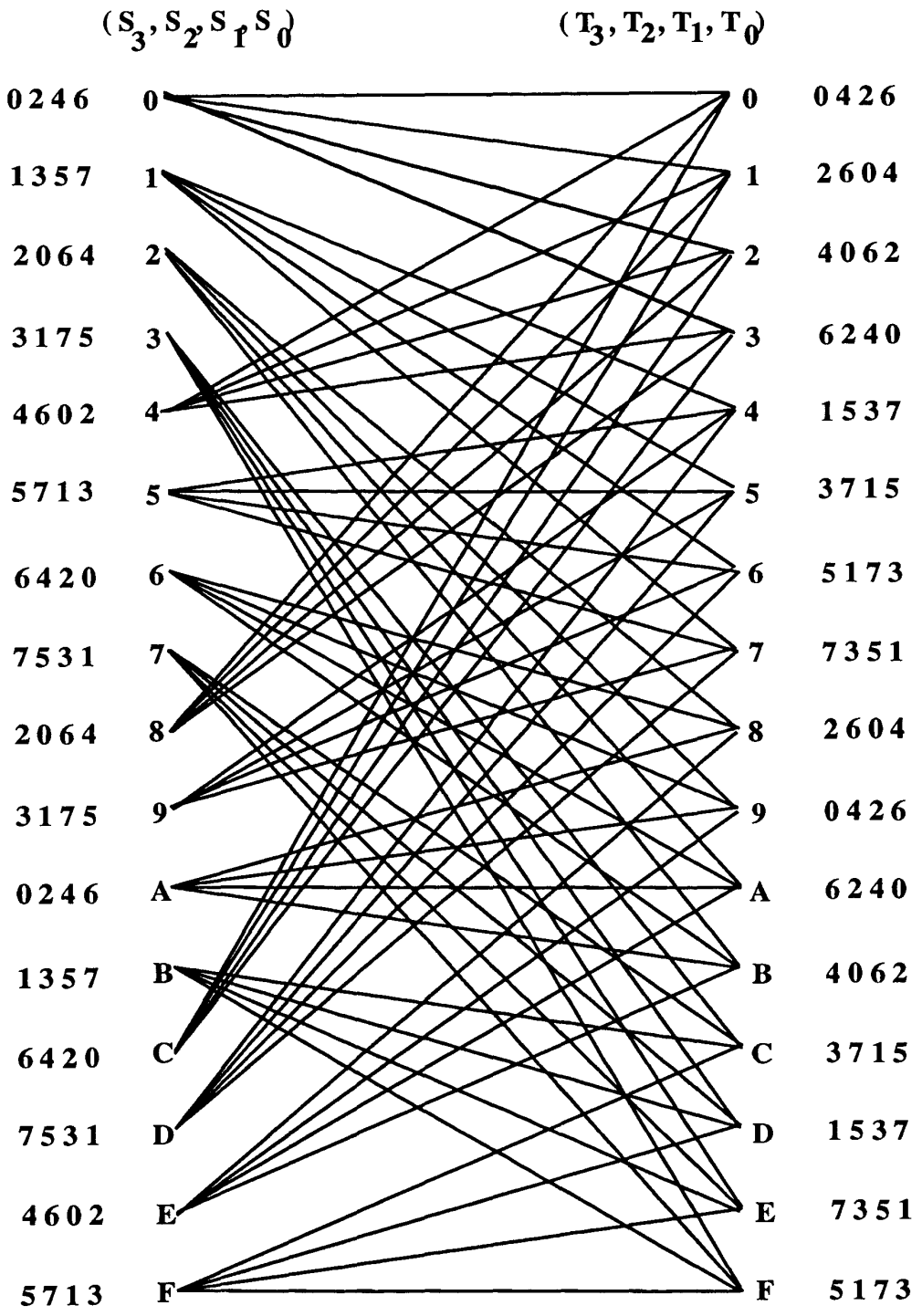

Figure 6.6-4: Trellis diagram

Figure 6.6-4 depicts the trellis diagram based on the finite state machine in Figure 6.6-2, and the one-to-one correspondence between (u_2 , u_1 , u_0) and the 4-dimensional cosets. In the figure, S = (S_3 , S_2 , S_1 , S_0) represents the current state, while T = (T_3 , T_2 , T_1 , T_0) represents the next state in the finite state machine. S is connected to T in the trellis diagram by a branch determined by the values of u_2 and u_1. The branch is labeled with the 4-dimensional coset specified by the values of u_2 , u_1 (and $u_0 = S_0$, see Figure 6.6-2). To make the trellis diagram more readable, the indices of the 4-dimensional coset labels are listed next to the starting and end points of the branches, rather than on the branches themselves. The leftmost label corresponds to the uppermost branch for each state. The trellis diagram is used when decoding the trellis code by the Viterbi algorithm.

6.6.4 Constellation encoder

For a given subchannel, the encoder selects an odd-integer point (X,Y) from the square-grid constellation based on the b bits $\{v_{b-1}, v_{b-2}, \ldots, v_1, v_0\}$. For convenience of description, the b bits $\{v_{b-1}, v_{b-2}, \ldots, v_1, v_0\}$ are identified with an integer label whose binary representation is $(v_{b-1}, v_{b-2}, \ldots, v_1, v_0)$. For example, for b=2, the four constellation points are labeled 0,1,2,3 corresponding to (v_1, v_0) = (0,0), (0,1), (1,0), (1,1) respectively.

6.6.4.1 Even values of b

For even values of b, the integer values X and Y of the constellation point (X,Y) are determined from the b bits $\{v_{b-1}, v_{b-2}, \ldots, v_1, v_0\}$ as follows. X is the odd integer with twos-complement binary representation $(v_{b-1}, v_{b-3}, \ldots, v_1, 1)$, while Y is the odd integer with twos-complement binary representation $(v_{b-2}, v_{b-4}, \ldots, v_0, 1)$. The MSBs v_{b-1} and v_{b-2} are the sign bits for X and Y respectively. Figure 6.6-5 shows example constellations for b = 2 and b= 4.

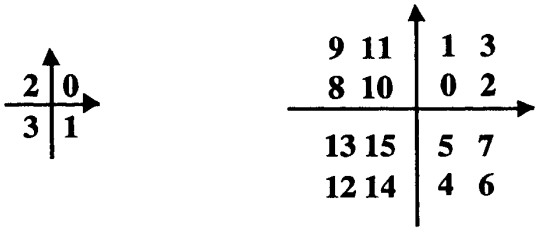

Figure 6.6-5: Constellation labels for b=2 and b=4

Note that the 4-bit constellation can be obtained from the 2-bit constellation by replacing each label n by the 2 x 2 block of labels:

4n+1	**4n+3**
4n	**4n+2**

The same procedure can be used to construct the larger even-bit constellations recursively.

The constellations obtained for even values of b are square in shape. Note that the LSBs $\{v_1, v_0\}$ represent the coset labeling of the constituent 2-dimensional cosets used in the 4-dimensional Wei trellis code.

6.6.4.2 Odd values of b, b ≤ 3

Figure 6.6-6 shows the constellation for the cases b = 1 and b= 3.

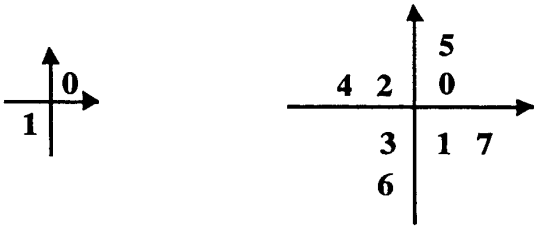

Figure 6.6-6: Constellation labels for b=1 and b=3

6.6.4.3 Odd values of b, b>3

If b is odd and larger than 3, the 2 msbs of X and the 2 msbs of Y are determined by the 5 msbs of the b bits. Let c = (b+1)/2, then X has twos-complement binary representation (X_c , X_{c-1} , v_{b-4} , v_{b-6} , v_{b-8} , ... , v_3 , v_1 , 1), and Y has twos-complement binary representation (Y_c , Y_{c-1} , v_{b-5} , v_{b-7} , v_{b-9} , ... , v_2 , v_0 , 1) where X_c and Y_c are the sign bits of X and Y respectively. The relationship between X_c , X_{c-1} , Y_c , Y_{c-1} and v_{b-1} , v_{b-2} , ... , v_{b-5} is shown in the following table.

v_{b-1} , v_{b-2} , ... , v_{b-5}	X_c , X_{c-1}	Y_c , Y_{c-1}
0 0 0 0 0	0 0	0 0
0 0 0 0 1	0 0	0 0
0 0 0 1 0	0 0	0 0
0 0 0 1 1	0 0	0 0
0 0 1 0 0	0 0	1 1
0 0 1 0 1	0 0	1 1
0 0 1 1 0	0 0	1 1
0 0 1 1 1	0 0	1 1
0 1 0 0 0	1 1	0 0
0 1 0 0 1	1 1	0 0
0 1 0 1 0	1 1	0 0
0 1 0 1 1	1 1	0 0
0 1 1 0 0	1 1	1 1
0 1 1 0 1	1 1	1 1
0 1 1 1 0	1 1	1 1
0 1 1 1 1	1 1	1 1
1 0 0 0 0	0 1	0 0
1 0 0 0 1	0 1	0 0
1 0 0 1 0	1 0	0 0
1 0 0 1 1	1 0	0 0
1 0 1 0 0	0 0	0 1
1 0 1 0 1	0 0	1 0
1 0 1 1 0	0 0	0 1
1 0 1 1 1	0 0	1 0
1 1 0 0 0	1 1	0 1
1 1 0 0 1	1 1	1 0
1 1 0 1 0	1 1	0 1
1 1 0 1 1	1 1	1 0
1 1 1 0 0	0 1	1 1
1 1 1 0 1	0 1	1 1
1 1 1 1 0	1 0	1 1
1 1 1 1 1	1 0	1 1

Table 6.6-3: Determining the top 2 bits of X and Y

Figure 6.6-7 shows the constellation for the case b = 5.

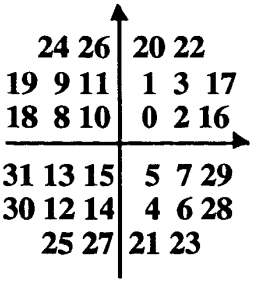

Figure 6.6-7: Constellation labels for b=5

The 7-bit constellation can be obtained from the 5-bit constellation by replacing each label n by the 2 x 2 block of labels:

4n+1	**4n+3**
4n	**4n+2**

Again, the same procedure can be used to construct the larger odd-bit constellations recursively. Note also that the LSBs $\{v_1,v_0\}$ represent the coset labeling of the constituent 2-dimensional cosets used in the 4-dimensional Wei trellis code.

***********EDITORIAL NOTE***********

Sub-clause 6.7 to 6.11
Status : Under Study (Oct./93 Interim Mtg.)
Cont. 93-190R1
Source: Amati

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6.7 Encoder (uncoded version)

An algorithmic constellation encoder is used to construct constellations with a maximum of 15 bits.

6.7.1 Bit extraction

Data bytes from the DMT symbol buffer are extracted according to a re-ordered bit allocation table b'_i, using the least-significant-bit-first convention. The number of bits per tone b'_i can take any non-negative integer values not exceeding 15, with the exception of $b'_i = 1$. For a given tone b'_i=b bits are extracted from the DMT symbol buffer, and these b bits form a binary word $\{v_{b-1}, v_{b-2}, \ldots, v_1, v_0\}$.

6.7.2 Constellation encoder

The constellation encoder requirements are as specified in 6.6.4.

6.8 Gain scaling

Each point (X_i,Y_i) or complex number $Z_i = X_i + jY_i$ output from the encoder is multiplied by the fine gain adjuster, g_i:

$$Z_i' = g_i Z_i$$

6.9 Modulation

6.9.1 Sub-carriers

6.9.1.1 Data sub-carriers

The Channel Analysis signal defined in Section 12.6 allows for a maximum of 255 carriers (at frequencies $n\Delta f$, n=1 to 255) to be used. If EC is used to separate downstream and upstream signals, then the lower limit on n is determined by the ADSL/POTS splitting filters; if FDM is used the lower limit is set by the down/up splitting filters. The cut-off frequencies of these filters are completely at the discretion of the manufacturer because in either case the range of usable n is determined during the Channel Estimation.

6.9.1.2 Pilot

Carrier #64 (f = 276 kHz) is reserved for a pilot; that is b_{64} = 0 and g_{64} = 1. ~~Randomization of the data on the pilot was proposed in 93-085, and will be defined after further study~~. Use of this pilot allows resolution of sample timing in a receiver modulo-8 samples. Therefore a gross timing error, which is an integer multiple of 8 samples, could still persist after a micro-interruption (e.g., a temporary short- circuit, open circuit or severe line hit); correction of these is made possible by the use of the synchronization symbol defined in Section 6.9.3

6.9.1.3 Nyquist frequency

The carrier at the Nyquist frequency (#256) may not be used for data; other possible uses are for further study.

6.9.2 Modulation by the Inverse Discrete Fourier Transform

512

The modulating transform defines the relationship between the 512 real values x_k and the Z_i'

$$x_k = \sum_{i=0}^{511} \exp(j\pi\, ki/32)\, Z_i' \quad \text{for } k = 0 \text{ to } 511$$

It should be noted that the encoder and scaler generate only 255 complex values of Z_i' (plus zero at d.c. and one real value if the Nyquist frequency is used). In order to generate real values of x_k these values must be augmented so that the vector Z' has Hermitian symmetry. That is,

$$Z_i' = Z_{512-i}'^* \qquad \text{for } i = 257 \text{ to } 511$$

***********EDITORIAL NOTE***********

Sub-clause 6.9.3 (Re length of the cyclic prefix)
Status : Under Study (Oct./93 Interim Mtg.)
Cont. 93-267
Source: Tellabs
Resolution: As suggested in the contribution, the section 6.8.2 in 93-190 was revised in the R1 version (93-190) text re the cylic prefix was removed.

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6.9.3 Synchronization symbol

The synchronization symbol permits recovery of the frame boundary after micro-interruptions that might otherwise force retraining.

The symbol rate, f_{symb} = 4kHz, the carrier separation, Δf = 4.3125 kHz, and the IDFT size, N = 512, are such that a cyclic prefix of 40 samples could be used. That is,

$$(512 + 40) \times 4.0 = 512 \times 4.3125 = 2208$$

The cyclic prefix is, however, shortened to 32 samples, and a synchronization symbol (with a nominal length of 544 samples) is inserted after every 68 data symbols. That is,

$$(512 + 32) \times 69 = (512 + 40) \times 68$$

The data pattern used in the synchronization symbol is the pseudo-random sequence PRD, (x_n, for n = 1 to 512) defined by

$x_n = 1$ for n = 1 to 9
$x_n = x_{n-4} + x_{n-9}$ for n =10 to 512

The bits are used as follows: the first pair of bits (x_1 and x_2) is used for the d.c.and Nyquist sub-carriers (the power assigned to them is, of course, zero, so the bits are effectively ignored); then the first and second bits of subsequent pairs are used to define the X_i and Y_i. for i = 1 to 255 as follows:

x_{2i+1}, x_{2i+2}	X_i, Y_i.
0, 0	+ +
0, 1	+ -
1, 0	- +
1, 1	- -

Bits 129 and 130, which modulate the pilot carrier, are also effectively discarded because the phase of the pilot may be determined by its own random pattern (see Section 6.9.1.2)

6.10 Cyclic prefix

The last 32 samples of the output of the IDFT (x_k for k = 481 to 512) are prepended to the block of 512 samples and read out to the DAC in sequence. That is, the subscripts, k, of the DAC samples in sequence are 481.....512,1.....512.

The cyclic prefix is used for data and synchronization symbols beginning with the RRATES1 segment of the initialization sequence, as defined in Section 12.6.2.1.

6.11 Digital-to-analog converter

6.11.1 Conversion rate

The conversion rate shall be 2208 kHz

6.11.2 Dynamic range

The maximum output signal of the DAC shall be such that the probability of the signal being clipped is no greater than 10^{-5}

6.11.3 Quantizing noise

The Signal-to-Quantizing Noise ratio (SQNR) of the DAC output is defined as the ratio of the rms value of a full-scale sine wave to the rms sum of all the non-fundamental signals generated up to half the conversion rate.

Over the frequency band 0 to 1104 kHz the SQNR of the DAC shall be no less than 78 dB.

7. ATU-R functional characteristics

**********EDITORIAL NOTE**********

Sub-clause 7.1 to 7.2
Status : Under Study (Oct./93 Interim Mtg.)
Cont. 93-191R1
Source: Amati
NOTE:

The following revised text is proposed for Sections 7.1 and 7.2 of the Draft Standard for DMT ADSL. Major changes relative to 93-191 include the following:

(a) changes in the data framing (including definition of synchronization control codes) to be consistent with contribution T1E1.4/93-119R2, "Revised Data Framing and Synchronization Conventions for DMT ADSL" (October 4, Alexandria, VA);
(b) addition of a data scrambler between the crc and FEC; and
(c) addition of an optional 576 kbit/s duplex data channel.

The following additional changes have been made for the November 1993 T1E1.4 meeting, and are indicated with revision marks:

(a) correction of table numbering in section 7.2;
(b) update of coding parameters in the first two rows of Table7.2-3;
(c) changes to the 3rd paragraph in Section 7.2.1.2.1;
(d) changes to 5th paragraph in Section 7.2.1.2.2; and
(e) change in nomenclature from "Loop Class" to "Transport Class" to be consistent with latest proposed text for Section 5.

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7.1 ATU-R input and output data interfaces

The functional data interfaces at the ATU-R are shown in Figure 7.1-1. Output interfaces for the high-speed downstream simplex bearer channels are designated AS0 through AS3; input/output interfaces for the duplex bearer channels are designated LS0 through LS2. There may also be a duplex interface for extending operations and, maintenance functions out to customer premises equipment; this interface is for further study.

The data rates of the input and output data interfaces at the ATU-R for the default configurations are specified in this section. The exact number of physical interfaces and the physical and electrical characteristics of these interfaces appear in Sections 9 and 16.

The total net bearer capacity that can be transmitted in the upstream direction (ATU-R to ATU-C) corresponds to the transport class as described in Section 5.4; the mix of data rates at the downstream simplex input interfaces is limited to a combination whose net bit rate does not exceed the net downstream simplex bearer capacity for the given transport class. Similarly, the rate of the duplex bearer at the LS0 interface and the availability of the LS1 and LS2 options correspond to the transport class as discussed in Section 5.4.

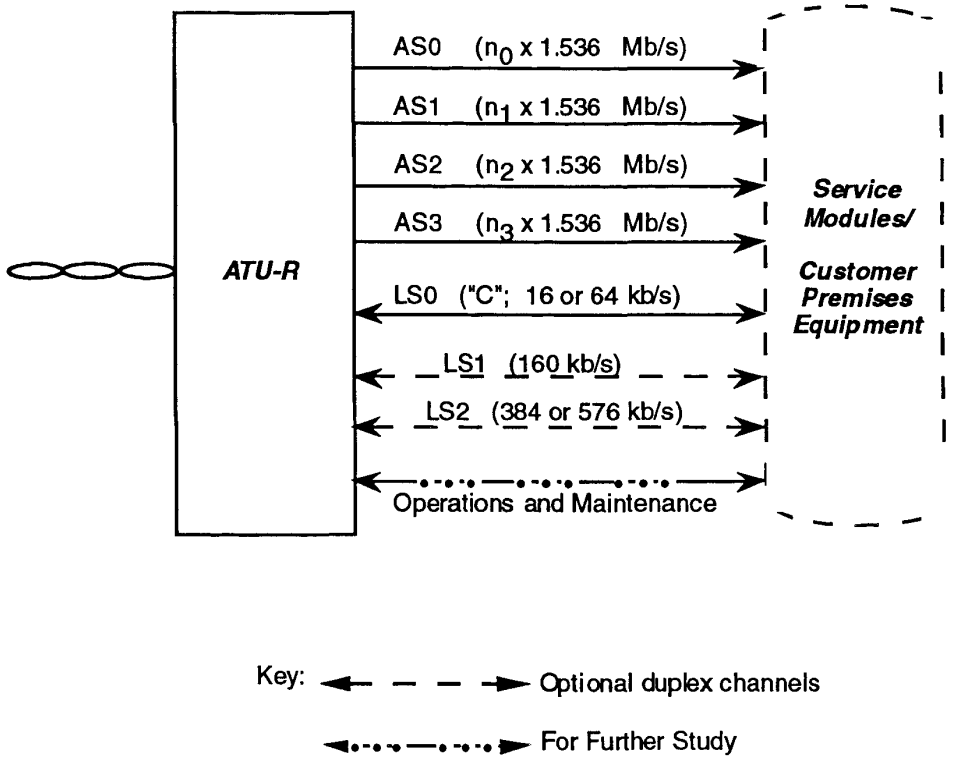


Figure 7.1-1. ATU-R Data Interfaces

7.1.1 Downstream simplex channels: transmit bit rates

The downstream simplex channels are transported in the downstream direction (ATU-C to ATU-R) only. The data interfaces at the ATU-R operate only as outputs.

7.1.1.1 Default Bearers based on 1.536 Mbit/s

There are four output interfaces at the ATU-R for the high-speed downstream simplex data channels: AS0, AS1, AS2 and AS3 (ASX in general). The data rates at these interfaces for the default configurations are n_x x 1.536 Mbit/s, where the allowed values of n_x are given in Table 7.1-1.

Table 7.1-1. Allowed Data Rates at the Downstream simplex Output Interfaces from the ATU-R, for Default Configurations (n x 1.536 Mbit/s Bearers)

Downstream simplex Channel	Data Rates	Allowed Values of n_x
AS0	0, 1.536, 3.072, 4.608, or 6.144 Mbit/s	n_0 = 0, 1, 2, 3, or 4
AS1	0, 1.536, 3.072 or 4.608 Mbit/s	n_1 = 0, 1, 2 or 3
AS2	0, 1.536 or 3.072 Mbit/s	n_2 = 0, 1 or 2
AS3	0 or 1.536 Mbit/s	n_3 = 0 or 1

7.1.1.2 Option for bearers based on 2.048 Mbit/s

In an optional configuration for bearers based on 2.048 Mbit/s data streams, there are three output interfaces at the ATU-R for the high-speed downstream simplex data channels: AS0, AS1 and AS2 (ASX in general). (Output interface AS3 does not exist or is not connected internally). The data rates at these interfaces are n_x x 2.048 Mbit/s, where the allowed values of n_x are given in Table 7.1-2.

Table 7.1-2. Allowed Data Rates at the Downstream simplex Output Interfaces from the ATU-R, Optional Configuration (2.048 Mbit/s Bearers)

Downstream simplex Channel	Data Rates	Allowed Values of n_x
AS0	0, 2.048, 4.096, or 6.144 Mbit/s	n_0 = 0, 1, 2 or 3
AS1	0, 2.048, or 4.096 Mbit/s	n_1 = 0, 1 or 2
AS2	0 or 2.048 Mbit/s	n_2 = 0 or 1

7.1.2 Duplex channels: transmit and receive bit rates

Both input and output data interfaces must be supplied at the ATU-R for the duplex bearers supported by the ADSL system.

Note: Two of the duplex channels are optional, as described in Section 5.2.2; the rate of the third duplex channel depends on the transport class, as defined in Section 5.2.1.

Table 7.1-3 shows the data rates that must be supported by both the input and output interfaces at the ATU-R for the duplex channels.

Table 7.1-3. Interface Data Rates for Duplex Channels

Duplex Channel	Data Rate
LS0 (Note 1)	16 or 64 kbit/s
LS1 (Note 2)	160 kbit/s
LS2	384 kbit/s or 576 kbit/s
Operations, Maintenance, and Control (Note 3)	TBD

Note 1: LS0 is also known as the "C" or Control Channel. It carries the signaling associated with the ASX data streams and the 384 kbit/s or 576 kbit/s duplex data stream. When LS1 transports ISDN BRA, the signaling for LS1 is contained within the ISDN BRA D channel; if LS1 is used to transport a non-ISDN BRA data stream, then its signaling will also be contained in the "C" channel.

Note 2: LS1 may be used to carry Basic Rate ISDN (2B + D + overhead, where overhead includes all functions normally associated with the ISDN "U" Interface (ANSI T1.601)).

Note 3: This interface is for further study.

7.2 Framing

Framing of the upstream signal (ATU-R transmitter) is specified in this section. The downstream framing (ATU-C transmitter) was specified in Section 6.2.

7.2.1 Data symbols

Figure 7.2-1 provides a functional block diagram of the ATU-R transmitter with reference points for data framing. Up to three duplex data channels are multiplexed and synchronized to the 4 kHz ADSL DMT symbol rate into two

separate data buffers (fast and interleaved). A cyclic redundancy check (crc), scrambling, and forward error correction (FEC) coding are applied to each data buffer separately. The interleaved data buffer is then passed through an interleaving function. The fast and interleaved data buffers are then combined into a data symbol that is input to the Trellis Encoder. After Trellis Coding, the data is modulated to produce an analog signal for transmission across the customer loop.

No bit-level framing pattern is inserted in the data symbols of the frame or superframe structure. DMT symbol, or frame, boundaries are delineated by the cyclic prefix inserted by the modulator (see Section 7.9). Superframe boundaries are determined by the synchronization symbol which is also inserted by the modulator and which carries no user data (see Section 7.8).

Due to the addition of FEC parity bytes and due to data interleaving, the data symbols (i.e., bit-level data prior to Trellis Encoding) have different structural appearance at the different reference points through the transmitter. As shown in Figure 7.2-1, the reference points for which data framing will be described in the following subsections are

(A) "Mux data frame", the multiplexed, synchronized data after the crc is inserted (synchronization is described in Section 7.2.2, crc is specified in Section 7.2.1.3);
mux data frames will be generated at a nominal 4 kHz rate (i.e., each 250 msec);

(B) "FEC output data frame", the data frame generated at the output of the FEC encoder at the DMT symbol rate, where an FEC block may span more than one DMT symbol period; and

(C) "Trellis Encoder input data frame", the data frame presented to the Trellis Coder.

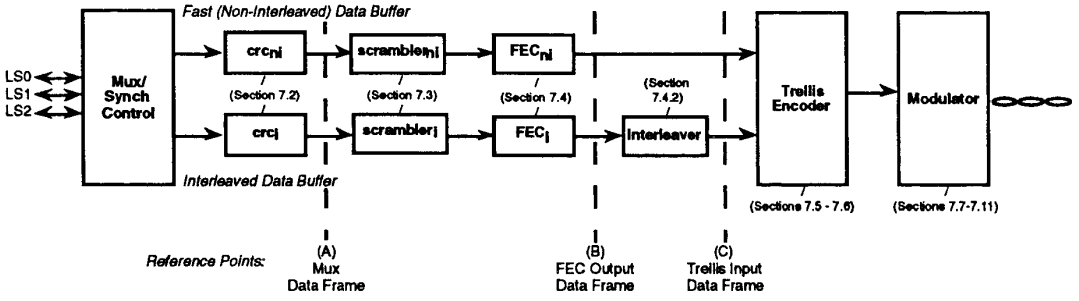


Figure 7.2-1. Reference Points for Data Framing, ATU-R Transmitter

7.2.1.1 Superframe structure

ADSL uses the superframe structure shown in Figure 7.2-2. Each superframe is composed of 68 ADSL data frames, numbered from 0 to 67, which are encoded and modulated into multicarrier (DMT) symbols, followed by a synchronization symbol that is inserted by the modulator (see Section 7.7) to establish superframe boundaries. The synchronization symbol carries no user or overhead bit-level data; from the bit-level and user data perspective, DMT symbols have a nominal period of 250 msec (4000 frames/sec). (The modulator transmits an extra synch symbol after every 68 data symbols, so that the transmitted DMT symbol rate is 68/69 * 250 msec). Each data frame within the superframe contains a fast data buffer and an interleaved data buffer. The size of each buffer depends on the assignment of bearer channels made during initialization (see Section 7.2.1 and 12.8.4). (On-line reassignment of bearer channels is for further study).

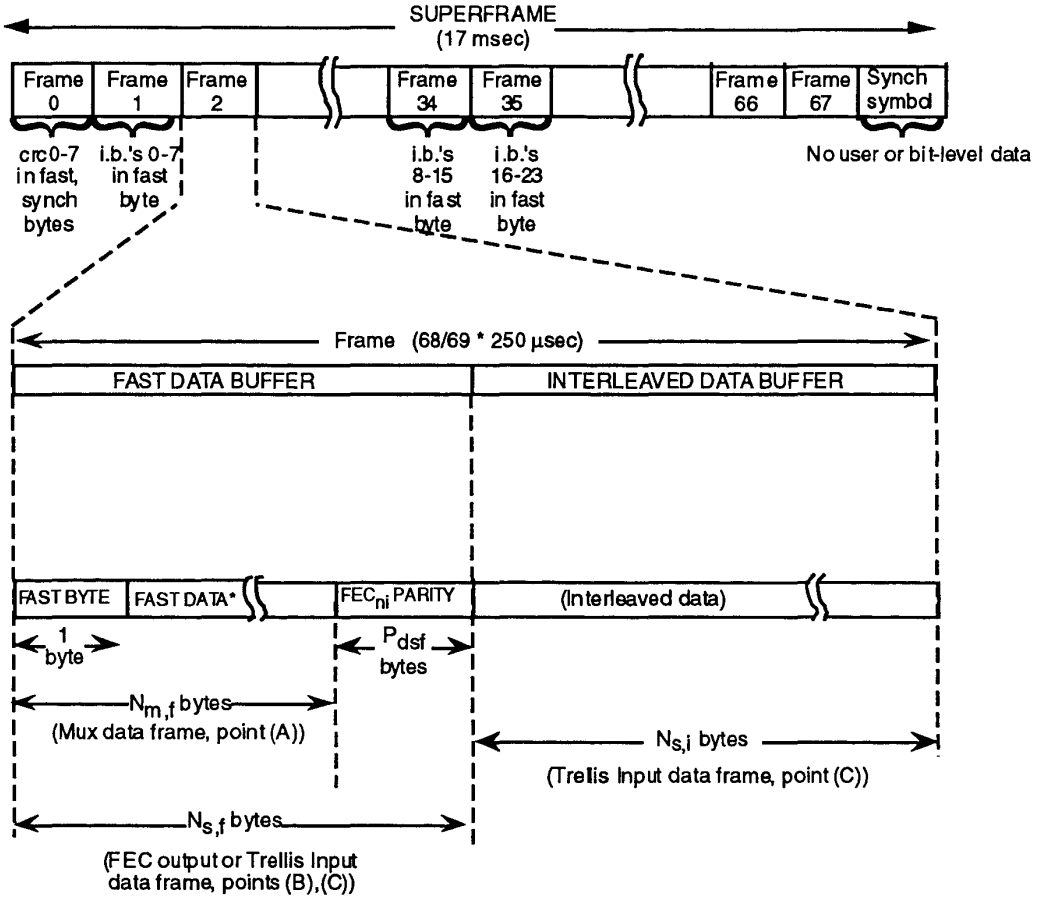


Figure 7.2-2. ADSL Superframe Structure, ATU-R Transmitter

Eight bits per ADSL superframe are reserved for the crc on the fast data buffer (crc0-crc7), and 24 indicator bits (ib0-ib23) are assigned for OAM functions. As shown in Figures 7.2-2 and 7.2-3, the "fast" byte of the fast data buffer carries the crc check bits in frame 0 and the fixed overhead bit assignments in frames 1, 34, and 35. The "fast" byte in other frames is assigned in even-/odd-frame pairs to either the eoc or to synchronization control of the bearer channels assigned to the fast buffer.

Note: Use of the "fast" byte to transport an OAM "EOC-like" data channel out to customer premises equipment is for further study (corresponds to certain functions at the interface labeled "Operations and Maintenance" in Figure 7.1-1).

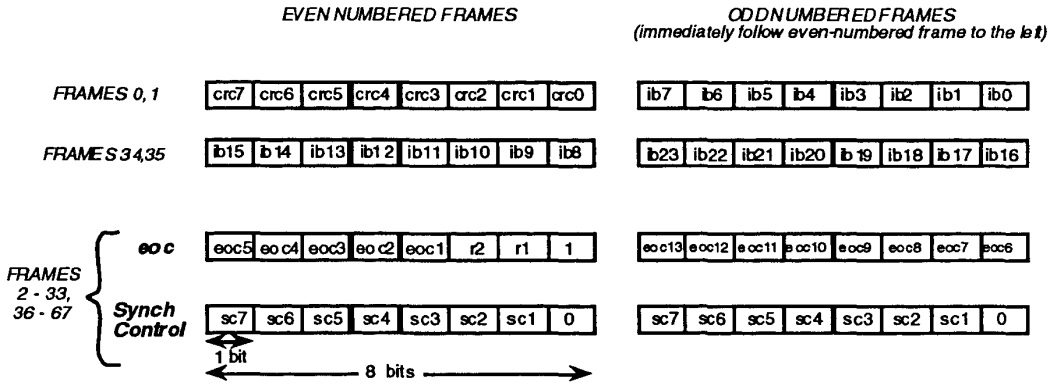


Figure 7.2-3. "FAST" Byte Format, ATU-R Transmitter, Fast Data Buffer

The indicator bit positions are defined in Table 7.2-1; the indicators themselves are defined in Section 11.3.

Table 7.2-1. Definition of indicator bits, ATU-R transmitter (Fast Data Buffer, Upstream direction)

Indicator Bit	Definition
ib0 - ib7	reserved for future use
ib8	febe-i
ib9	fecc-i
ib10	febe-ni
ib11	fecc-ni
ib12	los
ib13	rdi
ib14 - ib23	reserved for future use

If bit 0 of the "fast" byte in an even-numbered frame (other than frames 0 and 34) is "1", then the "fast" byte of that frame and the odd-numbered frame that immediately follows is used to carry a 13-bit "eoc frame", which is defined in Section 11.2 and in [1] as follows:

eoc1, eoc2	Address (11=ATU-R, 00=ATU-R, 01 and 10 reserved)
eoc3	Data/Mesage Indicator Bit: "0" = information field contains op code for ADSL eoc message, "1" = information field contains binary or ASCII data.
eoc4	Odd ("1") / Even ("0") byte indicator for multibyte transmission in data read or write mode
eoc5	Unspecified, set to 1 (reserved for future use) Note 1
eoc6 - eoc13	Information field.

Note 1: Use of eoc5 to designate an autonomous message or an indicator message from the ATU-R that does not affect the eoc protocol state is for further study.

The eoc protocol and message formats are described in Section 11.2.

If bit 0 of the "fast" byte in an even-numbered frame (other than frames 0 and 34) is "0", then the "fast" byte of that frame and the odd-numbered frame that immediately follows is used for synchronization control (the "fast" byte format for synch control is described in Section 7.2.2.1).

Eight bits per ADSL superframe are reserved for the crc on the interleaved data buffer (crc_i0-crc_i7). As shown in Figures 7.2-2 and 7.2-4, the "synch" byte of the interleaved data buffer carries the crc check bits in frame 0. In all other frames (1 through 67), the "synch" byte is used for synchronization control of the bearer channels assigned to the interleaved data buffer or it is used to carry an ADSL overhead control channel (this latter use is for further study). When any bearer data streams appear in the interleave buffer, then the ADSL overhead control channel data is carried in the LEX byte, and the "synch" byte designates when the LEX byte contains this channel's data and when it contains data bytes from the bearer data streams. When no bearer data streams are allocated to the interleave data buffer, i.e., all B_I(LSX) = 0, then the "synch" byte carries the ADSL overhead control channel data directly (LEX does not exist in the interleave buffer in this case). The format of the "synch" byte is described in Section 7.2.2.2.

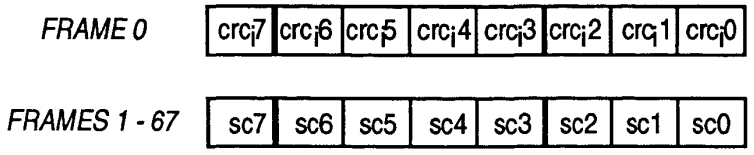


Figure 7.2-4. "Synch" Byte Format, ATU-R Transmitter Interleaved Data Buffer

7.2.1.2 Frame structure

Each frame of data will be encoded into a multicarrier symbol, as described in Sections 7.3 through 7.6. As was shown in Figure 7.2-1, each frame is composed of a fast data buffer and an interleaved data buffer, and the frame structure has a different appearance at each of the reference points (A, B, and C). The bytes of the fast buffer will be clocked into the Trellis Encoder first, followed by the bytes of the interleaved data buffer. Bytes are clocked least significant bit first.

The assignment of user data streams to the fast and interleaved buffers is configured during initialization (see Section 11.6) with the exchange of a B_F, B_I pair for each data stream, where B_F designates the number of bytes of a given data stream to allocate to the fast buffer, and B_I designates the number of bytes allocated to the interleaved data buffer.

The possible values of B_F, B_I for a given data signal X are:

1) To place data signal X in the fast data buffer:
   $B_F(X) = 0$, $B_I(X)$ = Data Rate of X (bits/s) / 32000.
2) To place data signal X in the interleaved data buffer:
   $B_F(X)$ = Data Rate of X (bits/s) / 32000, $B_I(X) = 0$.

The seven possible B_F, B_I pairs are
B_F(LSX), B_I(LSX) for X = 0, 1 and 2, for the duplex channels.

Default configurations (i.e., sets of B_F, B_I pairs) for the four possible transport classes is given in Table 7.2-2.

Note: On-line reconfiguration (e.g., changing the mix of downstream simplex data channel rates, reallocation of user data streams between fast and interleaved data buffers) is for further study.

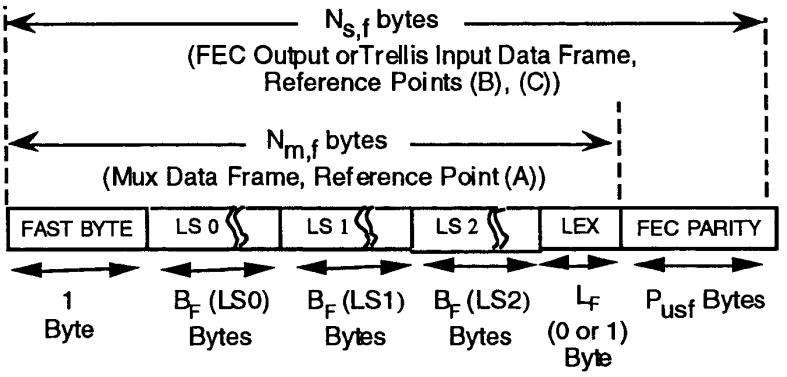
Table 7.2-2. Default Fast and Interleaved Data Buffer Allocations for ATU-R Transmitter

Signal	B_I (Interleaved Data Buffer) for Transport Classes 1 or 2M-1 / 2 or 2M-2 / 3 / 4 or 2M-3	B_F (Fast Data Buffer) for Transport Classes 1 or 2M-1 / 2 or 2M-2 / 3 / 4 or 2M-3
LS0	2 / 2 / 2 / 1 (Note 1)	0 / 0 / 0 / 0
LS1	0 / 0 / 0 / 0	5 / 0 / 0 / 5
LS2	0 / 0 / 0 / 0	12 / 12 / 12 / 0

Note 1: In the case of Transport Class 4 or 2M-3, $B_F(LS0) = 1$ or $B_I(LS0) = 1$ indicates a 16 kbit/s "C" channel, which is carried entirely within the synchronization control overhead as described in Section 7.2.2, so that the LS0 sub-channel does not appear as a separate byte within the ADSL frame.

7.2.1.2.1 Fast data buffer

The frame structure of the fast data buffer is shown in Figure 7.2-5 for the three reference points that were defined in Figure 7.2-1.



$$N_{m,f} = 1 + \sum_{j=0}^{2} B_F(LS_j) + L_F, \qquad N_{s,f} = N_{m,f} + P_{usf}$$

$$\text{where } L_F = \begin{cases} 0, & \sum_{j=0}^{2} B_F(LS_j) = 0, \\ 1 & \text{otherwise.} \end{cases} \qquad \text{where } P_{usf} = \#\text{ FEC Parity Bytes.}$$

Figure 7.2-5. Fast Data Buffer, ATU-R Transmitter

At reference point A, the Mux Data Frame, the fast buffer always contains at least the "fast" byte. This is followed by $B_F(LS0)$ bytes of channel LS0, then $B_F(LS1)$ bytes of channel LS1, and $B_F(LS2)$ bytes of channel LS2,and if any $B_F(LSX)$ is non-zero, an LEX byte.

P_{usf} FEC check bytes are added to the Mux data frame (reference point A) to produce the FEC output data frame (reference point B), where P_{usf} is given in the RATES1 signal options received from the ATU-C during Initialization (see Section 12). For the default configurations given in Table7.2-2, $P_{usf} = 4$. There always exists only one FEC codeword per symbol, so that the Trellis input data frame (reference point C) is identical to the FEC output data frame (reference point B).

7.2.1.2.2 Interleaved data buffer

The frame structure of the interleaved data buffer is shown in Figure 7.2-6 for the three reference points that were defined in Figure 7.2-1.

At reference point A, the Mux Data Frame, the interleaved data buffer always contains at least the "synch" byte. The rest of the buffer is built in the same manner as the fast buffer, substituting B_I in place of B_F. The length of each Mux data frame is $N_{m,i}$ bytes, where $N_{m,i}$ is defined in Figure 7.2-6.

The FEC coder will take in S Mux Data Frames and append P_{usi} FEC parity bytes to produce the FEC codeword of length $N_{FEC,i} = S * N_{m,i} + P_{usi}$. The FEC output data frames will contain $N_{s,i} = N_{FEC,i}/S$ bytes. When S > 1, then for the S frames in an FEC codeword, the FEC output Data Frame (reference point B) will partially overlap two Mux Data Frames for all but the last frame, which will contain the P_{usi} FEC parity bytes.

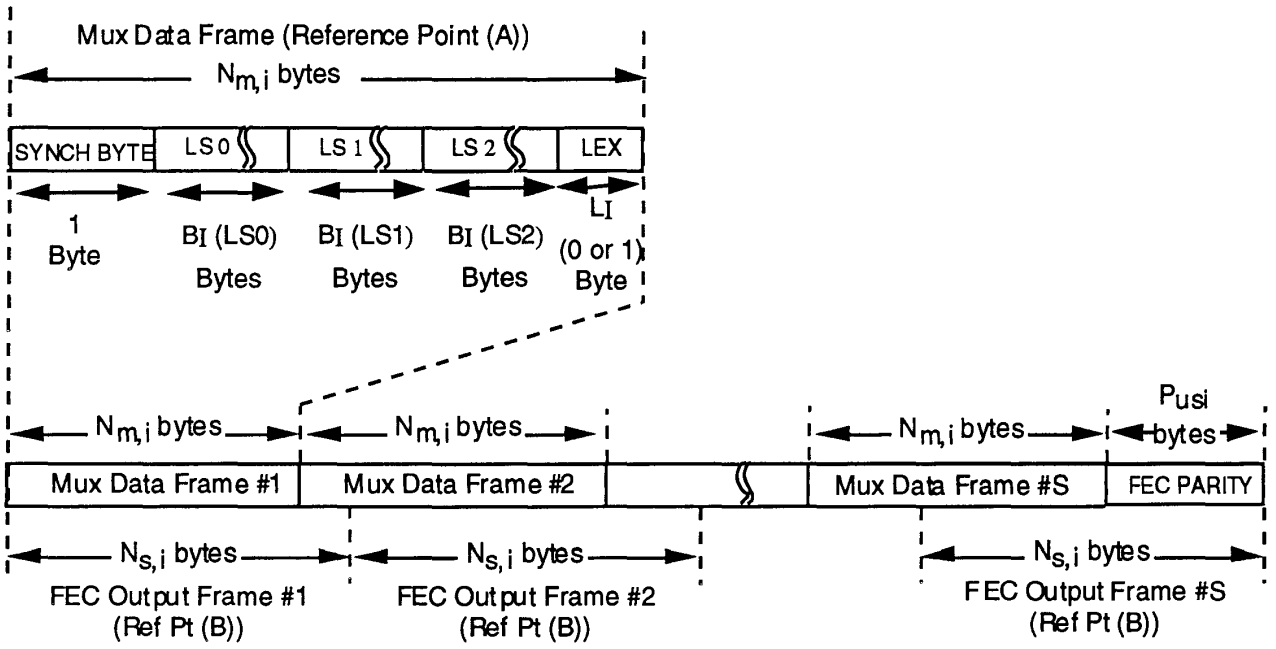
The FEC output data frames are interleaved to a specified interleave depth. The interleaving process (see Section 7.4.2) delays each byte of a given FEC output data frame a different amount, so that the Trellis input data frames will contain bytes from many different FEC data frames. At reference point A in the transmitter, mux data frame 0 of the interleaved data buffer is aligned with the ADSL superframe and mux data frame 0 of the fast data buffer (this is not true at reference point C). At the receiver, the interleaved data buffer will be delayed approximately 16 msec with respect to the fast data buffer and frame 0 (containing the crc bits for the interleaved data buffer) will appear a fixed number of frames after the beginning of the receiver superframe (the exact delay will depend on the de-interleaver implementation, so is left to the vendor).

The FEC coding overhead, the number of symbols per FEC codeword, and the interleave depth are given in the RATES1 options received from the ATU-C during Initialization (see Section 12). For the default configurations (i.e, for LS0 allocated to the interleave buffer; LS1 and LS2 allocated to the fast buffer) listed in Table 7.2-2, the coding parameters are given in Table 7.2-3.

Table 7.2-3. Default FEC Coding Parameters and Interleave Depth, ATU-R Transmitter

	P_{usi} (FEC Parity Bytes)	S (symbols per codeword)	Interleave Depth (FEC codewords) (see Note)
Transport Classes1, 2M-1	16	8	8
Transport Classes2, 3, 2M-2	16	16	4
Transport Classes4, 2M-3	16	16	4
Synch Byte Only	4	4	16

Note: Interleave depths effect 16 msec latency for the interleave/deinterleave function.



$$N_{m,i} = 1 + \sum_{j=0}^{2} B_I(LS_j) + L_I,$$

where $L_I = \begin{cases} 0, & \sum_{j=0}^{2} B_I(LS_j) = 0, \\ 1 & \text{otherwise.} \end{cases}$

$$N_{s,i} = (S * N_{m,i} + P_{usi}) / S,$$

where P_{usi} = # FEC Parity Bytes,
and S = # DMT symbols per FEC codeword.

Figure 7.2-6: *Interleaved Data Buffer, ATU-R Transmitter*

7.2.1.3 Cyclic redundancy check (crc)

Two cyclic redundancy checks (crc's) are generated for each superframe: one for the fast data buffer and one for the interleaved data buffer. Eight bits per buffer type (fast or interleaved) per superframe are allocated to the crc function. The crc bits are

a) The "fast byte" (8 bits) of frame 0 in the fast data buffer, and
b) the "synch byte" (8 bits) of frame 0 in the interleaved data buffer.

The crc generating polynomial for both the fast data buffer and the interleaved data buffer is

$$D^8 + D^4 + D^3 + D^2 + 1,$$

where + denotes modulo 2 summation.

Each crc's shift register cells are set to 1 at the beginning of the superframe.
The bits covered by the crc include

1) For the fast data buffer:
   Frame 0: LSX bytes (X = 0, 1, 2), followed by the LEX byte.
   All other frames: "fast" byte, followed by LSX bytes (X = 0, 1, 2), and LEX byte.
2) For the interleaved data buffer:
   Frame 0: LSX bytes (X = 0, 1, 2), followed by and LEX byte.
   All other frames: "synch" byte, followed by LSX bytes (X = 0, 1, 2), and LEX byte.

Each byte will be clocked into the crc least significant bit first.

Note that the crc field length will vary with the allocation of bytes to the fast and interleaved data buffers (the number of bytes in LSX vary according to the BF, BI pairs; LEX is present in a given buffer only if at least one LSX is allocated to that buffer).

[Note: Due to the flexibility in assignment of bearer channels to the fast and interleaved data buffers, crc field lengths over an ADSL superframe will vary from approximately 530 bits to approximately 116,000 bits; typical ranges will be TBD to TBD.]

7.2.2 Synchronization

The input data streams are synchronized to the ADSL clock using the synchronization control byte and the LEX byte. Forward-error-correction coding is always applied to the synchronization control byte(s).

7.2.2.1 Synchronization for the fast data buffer

Synchronization control for the fast data buffer can occur in frames 2 through 33 and 36 through 67 of an ADSL superframe as described in Section 7.2.1.1, where the "fast" byte may be used as the synchronization control byte.

The format of the "fast" byte when used as synchronization control for the fast data buffer is *given in the following table:*

sc7-sc4	not used	
sc3, sc2	LSX channel designator	"00" : channel LS0 "01" : channel LS1 "10" : channel LS2 "11" : do nothing to any LSX channel
sc1	Synchronization control for the designated LSX channel	"1" : add LEX byte to designated LSX channel "0" : delete last byte from designated LSX channel
sc0	Synch/eoc designator	"0" : perform synchronization control as indicated in sc7-sc1 "1" : this byte of current (even-numbered) frame and of frame that immediately follows is an eoc frame

No synchronization action is to be taken for frames in which the "fast" byte is used for crc, fixed indicator bits or eoc.

7.2.2.2 Synchronization for the Interleaved Data Buffer

Synchronization control for the interleaved data buffer can occur in frames 2 through 67 of an ADSL superframe as described in Section 7.2.1.1, where the "synch" byte may be used as the synchronization control byte.

The format of the "synch" byte when used as synchronization control for the interleaved data buffer is *given in the following table:*

sc7-sc4	not used	
sc3, sc2	LSX channel designator	"00" : channel LS0 "01" : channel LS1 "10" : channel LS2 "11" : do nothing to any LSX channel
sc1	Synchronization control for the designated LSX channel	"1" : add LEX byte to designated LSX channel "0" : delete last byte from designated LSX channel
sc0	Synch/aoc designator	"0" : perform synchronization control as indicated in sc7-sc1 "1" : LEX byte carries ADSL overhead control channel data

No synchronization action is to be taken during frame 0, where the "synch" byte is used for crc.

**********EDITORIAL NOTE**********

Sub-clause 7.3 to 7.6
Status : ~~Under Study~~ (Oct./93 Interim Mtg.)
Cont. ~~93-192R1~~
Source: Amati

Prov. Agree.

Note: Sub-clause 7.6 remains under study until the issue of what Trellis Code Modulation scheme(s) are agreed to in future. See the editorial note preceding sub-clause 7.7.

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7.3 Scramblers

The binary data streams output from the fast and interleaved buffers are scrambled separately using the following algorithm for both:

$d_n' = d_n + d_{n-5}' + d_{n-23}'$

where + indicates modulo-two addition, d_n is the n-th output from the fast or interleaved buffer, and d_n' is the corresponding n-th output from either of the scramblers.

7.4 Forward error correction

7.4.1 Reed-solomon coding

R redundant check bytes $C_{R-1}, C_{R-2}, \ldots, C_1, C_0$ are appended to K message bytes $M_{K-1}, M_{K-2}, \ldots, M_1, M_0$ to form a Reed-Solomon code word of size N = K + R bytes. The check bytes are computed from the message byte using the equation:

$C(z) = M(z)\, z^R$ modulo $G(z)$

where $C(z) = C_{R-1}\, z^{R-1} + C_{R-2}\, z^{R-2} + \ldots + C_1\, z + C_0$ is the check polynomial,

$M(z) = M_{K-1}\, z^{K-1} + M_{K-2}\, z^{K-2} + \ldots + M_1\, z + M_0$ is the message polynomial,

and $G(z) = \prod (z + {}^{i})$ is the generator polynomial of the Reed-Solomon code, where the index of the product runs from i = 0 to R-1. In other words, C(z) is the remainder obtained from dividing $M(z)\, z^R$ by G(z). The arithmetic is performed in the Galois Field GF(2^8), where is a primitive element which satisfies the primitive binary polynomial $x^8 + x^4 + x^3 + x^2 + 1$. A data byte ($d_7, d_6, \ldots, d_1, d_0$) is identified with the Galois Field element

$d_7\, {}^{7} + d_6\, {}^{6} + \ldots + d_1\, {} + d_0$

The number of check bytes R, and the codeword size N vary, as explained in the earlier section on framing.

7.4.2 Interleaving

The Reed-Solomon codewords in the interleave buffer are convolutionally interleaved. The interleaving depth D varies, as explained in the earlier section on framing, but it is always a power of 2. Convolutional interleaving is defined by the rule:

Each of the N bytes X_0 , X_1 , ... , X_{N-1} in a Reed-Solomon codeword is delayed by an amount which varies linearly with the byte index. More precisely byte X_i (with index i) is delayed by (D-1) * i bytes, where D is the interleave depth.

An example for N = 5, D = 2 is shown in the following table where X^j_i denotes the i-th byte of the j-th codeword.

Inter-leaver Input	X^j_0	X^j_1	X^j_2	X^j_3	X^j_4	X^{j+1}_0	X^{j+1}_1	X^{j+1}_2	X^{j+1}_3	X^{j+1}_4
Inter-leaver Output	X^j_0	X^{j-1}_3	X^j_1	X^{j-1}_4	X^j_2	X^{j+1}_0	X^j_3	X^{j+1}_1	X^j_4	X^{j+1}_2

Table 7.4-1: Convolutional Interleaving Example for N = 5, D =2

With the above mentioned rule, and the chosen interleaving depths (powers of 2), the output bytes from the interleaver always occupy distinct time slots as long as N is odd. When N is even, a dummy byte is added at the beginning of the codeword at the input to the interleaver. The resultant odd-length codeword is then convolutionally interleaved, and the dummy byte then removed from the output of the interleaver.

7.5 Tone ordering

A DMT time-domain signal has a high peak-to-average ratio (its amplitude distribution is almost Gaussian), and large values may be clipped by the digital-to-analog converter. The error signal caused by clipping can be considered an additive negative impulse for the time sample that was clipped. The clipping error power is equally distributed across all tones in the symbol in which clipping occurs. It therefore is most likely to cause errors on those tones that, in anticipation of a higher received SNR, have been assigned the largest number of bits (and therefore have the densest constellations). These occasional errors can be reliably corrected by the FEC coding if the tones with the largest number of bits have been assigned to the interleave buffer.

The numbers of bits and the relative gains to be used for every tone are calculated in the ATU-C receiver, and sent back to the ATU-R according to a defined protocol (see later section). The pairs of numbers are typically stored, in ascending order of frequency or tone number i, in a Bit and Gain table.

The "tone-ordered" encoding assigns the first B_F bytes ($8B_F$ bits) from the symbol buffer (see earlier section on framing) to the tones with the smallest number of bits assigned to them, and the remaining B_I bytes ($8B_I$ bits) to the remaining tones.

The ordered bit table b'_i is based on the original bit table b_i as follows:

For k = 0 to 15 { From the bit table, find the set of all i with the number of bits per tone b_i = k
Assign b_i to the ordered bit allocation table in ascending order of i }

A complementary de-ordering procedure must be performed in the ATU-C receiver. It is not necessary, however, to send the results of the ordering process to the receiver because the bit table was originally generated in the ATU-C, which therefore has all information necessary to perform the de-ordering.

**********EDITORIAL NOTE**********

Sub-clause 7.6
Status : Under Study (Oct./93 Interim Mtg.)
Cont. 93-265 (with supporting rationale in 93-264)
Source: Orckit and PairGain

Note: Proposes text that deals with Trellis Coded Modulation (TCM) scheme that is believed to be not patented. The issue of what TCM scheme will be in the standard remains unresolved. The objective is to resolve the issue by the Jan./94 Interim meeting.

In the mean time, the text associatted with the use of the Wei TCM scheme is provided in the draft standard. This could change in the future dependent on what the final resolution of this issue is.

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7.6 Trellis encoder

Block processing of Wei's 16-state 4-dimensional trellis code is included to improve system performance. An algorithmic constellation encoder is used to construct constellations with a maximum of 15 bits.

7.6.1 Bit extraction

Data bytes from the DMT symbol buffer are extracted according to a re-ordered bit allocation table b'_i, using the least-significant-bit-first convention. Due to the 4-dimensional nature of the recommended code, the extraction is based on pairs of consecutive b'_i, rather than on individual ones, as in the non-trellis-coded case. Furthermore, due to the constellation expansion associated with trellis coding, the bit allocation table b'_i specifies the number of coded bits per tone. The bit allocation algorithm during initialization iterates directly on the number of coded bits per tone. The number of bits per tone b'_i can take any non-negative integer values not exceeding 15, with the exception of $b'_i = 1$. Given a pair (x,y) of consecutive b'_i, x+y-1 bits (reflecting a constellation expansion of 1 bit per 4 dimensions, or half bit per tone) are extracted from the DMT symbol buffer. These $z = x+y-1$ bits ($t_z , t_{z-1} , \ldots , t_1$) are used to form the binary word u as shown in Table 7.6-1. The tone ordering procedure ensures $x \pounds y$. Single-bit constellations are not allowed because they can be replaced by 2-bit constellations with the same average energy. Please refer to section 6.6.2 for the reason behind the special form of the word u for the case $x = 0 , y > 1$.

Condition	Binary Word / Comment
$x > 1 , y > 1$	$u = (t_z , t_{z-1} , \ldots , t_1)$
$x = 1 , y \geq 1$	Condition not allowed
$x = 0 , y > 1$	$u = (t_z , t_{z-1} , \ldots , t_2 , 0 , t_1 , 0)$
$x = 0 , y \pounds 1$	Bit extraction not necessary, no message bits being sent

Table 7.6-1: Forming the Binary Word u

The final two 4-dimensional symbols in the DMT symbol are chosen to force the trellis state to the zero state. For each of these symbols, the 2 lsbs of u are pre-determinded, and only x+y-3 bits are extracted from the DMT symbol buffer.

7.6.2 Bit conversion

The binary word $u = (u_{z'} , u_{z'-1} , \ldots , u_1)$ determines two binary words $v = (v_{z'-y} ,\ldots,v_0)$ and $w = (w_{y-1},\ldots,w_0)$, which are used to look up two constellation points in the encoder constellation table. For the usual case, x>1, y>1, then $z' = z = x+y-1$. Thus in this case v and w contain x and y bits respectively. For the special case, $x = 0$, $z' = z+2$

= y-1. In the latter case, v = (v_1,v_0) = 0 while w = (w_1,w_0). The bits (u_3,u_2,u_1) determine (v_1 , v_0) and (w_1 , w_0) according to Figure 7.6-1 where the sign ≈ denotes exclusive-or.

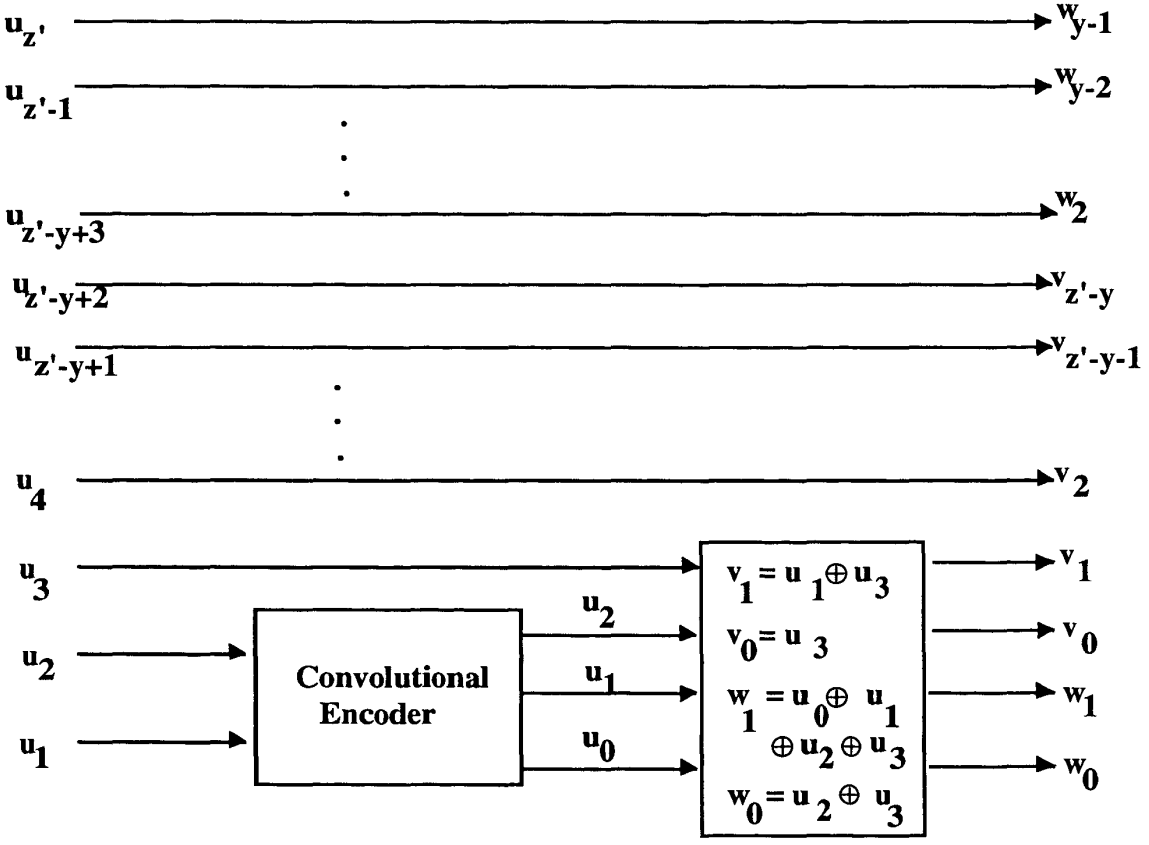

Figure 7.6-1: Conversion of u to v and w

The convolutional encoder shown in Figure 7.6-1 is a systematic encoder (i.e. u_1 and u_2 are passed through unchanged) as depicted in Figure 7.6-2. The states (S_3 , S_2 , S_1 , S_0) are used to label the states of the trellis diagram shown in Figure 7.6-4. The initial state (S_3 , S_2 , S_1 , S_0) is the zero state (0, 0, 0, 0) at the beginning of a DMT symbol period.

The remaining bits of v and w are obtained respectively from the less significant and more significant part of ($u_{z'}$, $u_{z'-1}$, ... , u_4). When x>1, y>1, v = ($u_{z'-y+2}$, $u_{z'-y+1}$, ... , u_4 , v_1 , v_0) and w = ($u_{z'}$, $u_{z'-1}$, ... , $u_{z'-y+3}$, w_1 , w_0). When x = 0, the bit extraction and conversion algorithms have been judiciously designed so that v_1 = v_0 = 0.

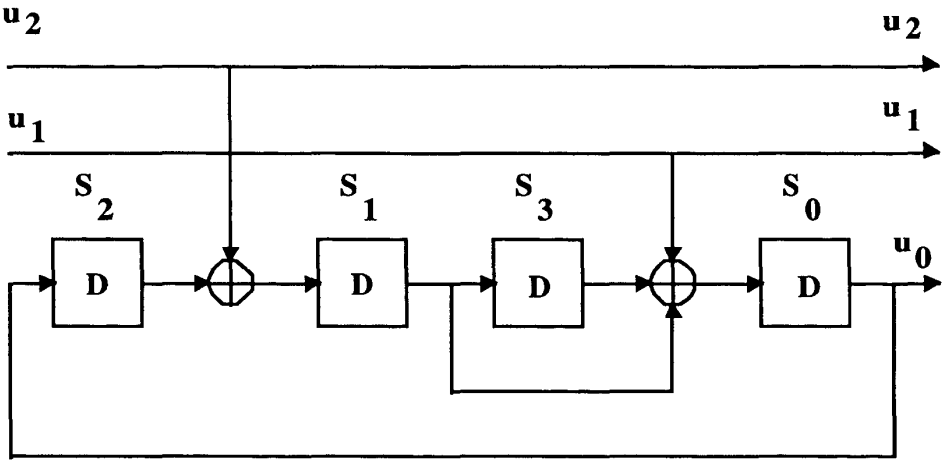

Figure 7.6-2: Finite State Machine for Wei's Encoder

In order to force the final state to the zero state (0,0,0,0), the 2 lsbs u_1 and u_2 of the final two 4-dimensional symbol in the DMT symbol are constrained to $u_1 = S_1 + S_3$, and $u_2 = S_2$, where '+' denotes exclusive-or.

7.6.3 Coset partition and trellis diagram

In a TCM system, the expanded constellation is labeled and partitioned into subsets using a technique called mapping by set-partitioning. These subsets are also called cosets. The four-dimensional cosets in Wei's code can each be written as the union of two Cartesian products of two 2-dimensional cosets. For example, $C_4^0 = (C_2^0 x C_2^0) U (C_2^3 x C_2^3)$. The four constituent 2-dimensional cosets, denoted by C_2^0, C_2^1, C_2^2, C_2^3, shown in Figure 7.6-3.

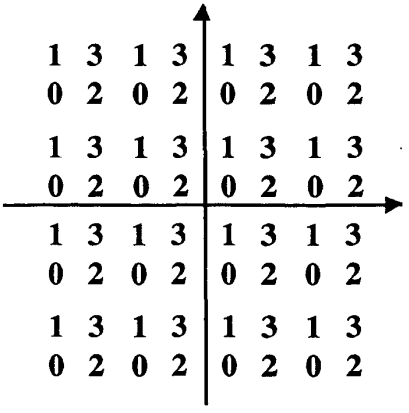

Figure 7.6-3: Constituent 2-dimensional cosets for Wei's code

The encoding algorithm guarantees that the 2 LSBs of a constellation point equals the index i of the 2-dimensional coset C_2^i in which the constellation point lies. The bits (v_1 , v_0) and (w_1 , w_0) are in fact the binary representations of these indices.

The three bits (u_2 , u_1 , u_0) are used to select one of the 8 possible four-dimensional cosets. The 8 cosets are labeled C_4^i where i is the integer with binary representation (u_2,u_1,u_0). The additional bit u_3 (seeFigure 7.6-1)

determines which of the two Cartesian products of 2-dimensional cosets in the 4-dimensional coset is chosen. The relationship is shown in Table 7.6-2. The bits (v_1,v_0) and (w_1,w_0) are computed from (u_3 , u_2 , u_1 , u_0) using the linear equations given inFigure 7.6-1.

4-D Coset	u_3 u_2 u_1 u_0	v_1 v_0	w_1 w_0	2-D Cosets
C_4^0	0 0 0 0 1 0 0 0	0 0 1 1	0 0 1 1	$C_2^0 \times C_2^0$ $C_2^3 \times C_2^3$
C_4^4	0 1 0 0 1 1 0 0	0 0 1 1	1 1 0 0	$C_2^0 \times C_2^3$ $C_2^3 \times C_2^0$
C_4^2	0 0 1 0 1 0 1 0	1 0 0 1	1 0 0 1	$C_2^2 \times C_2^2$ $C_2^1 \times C_2^1$
C_4^6	0 1 1 0 1 1 1 0	1 0 0 1	0 1 1 0	$C_2^2 \times C_2^1$ $C_2^1 \times C_2^2$
C_4^1	0 0 0 1 1 0 0 1	0 0 1 1	1 0 0 1	$C_2^0 \times C_2^2$ $C_2^3 \times C_2^1$
C_4^5	0 1 0 1 1 1 0 1	0 0 1 1	0 1 1 0	$C_2^0 \times C_2^1$ $C_2^3 \times C_2^2$
C_4^3	0 0 1 1 1 0 1 1	1 0 0 1	0 0 1 1	$C_2^2 \times C_2^0$ $C_2^1 \times C_2^3$
C_4^7	0 1 1 1 1 1 1 1	1 0 0 1	1 1 0 0	$C_2^2 \times C_2^3$ $C_2^1 \times C_2^0$

Table 7.6-2: Relation between 4-dimensional and 2-dimensional cosets

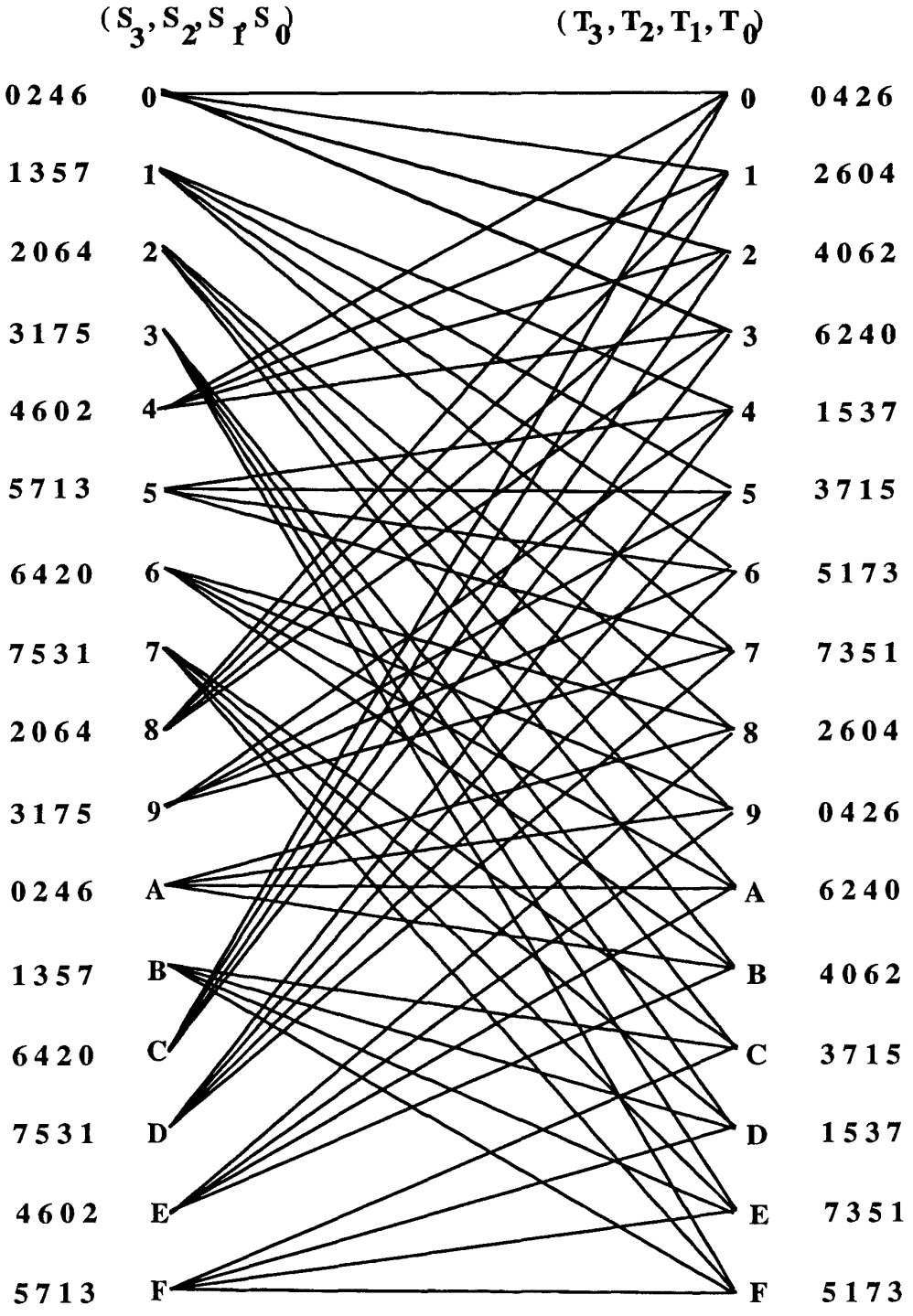

Figure 7.6-4: Trellis diagram

Figure 7.6-4 depicts the trellis diagram based on the finite state machine inFigure 7.6-2, and the one-to-one correspondence between (u_2 , u_1 , u_0) and the 4-dimensional cosets. In the figure, S = (S_3 , S_2 , S_1 , S_0)

represents the current state, while T = (T_3 , T_2 , T_1 , T_0) represents the next state in the finite state machine. S is connected to T in the trellis diagram by a branch determined by the values of u_2 and u_1. The branch is labeled with the 4-dimensional coset specified by the values of u_2 , u_1 (and $u_0 = S_0$, seeFigure 7.6-2). To make the trellis diagram more readable, the indices of the 4-dimensional coset labels are listed next to the starting and end points of the branches, rather than on the branches themselves. The leftmost label corresponds to the uppermost branch for each state. The trellis diagram is used when decoding the trellis code by the Viterbi algorithm.

7.6.4 Constellation encoder

For a given subchannel, the encoder selects an odd-integer point (X,Y) from the square-grid constellation based on the b bits {v_{b-1}, v_{b-2}, ... , v_1, v_0}. For convenience of description, the b bits {v_{b-1}, v_{b-2}, ... , v_1, v_0} are identified with an integer label whose binary representation is (v_{b-1}, v_{b-2}, ... , v_1, v_0) . For example, for b=2, the four constellation points are labeled 0,1,2,3 corresponding to (v_1, v_0) = (0,0), (0,1), (1,0), (1,1) respectively.

7.6.4.1 Even values of b

For even values of b, the integer values X and Y of the constellation point (X,Y) are determined from the b bits {v_{b-1}, v_{b-2}, ... , v_1, v_0} as follows. X is the odd integer with twos-complement binary representation (v_{b-1}, v_{b-3}, ... , v_1, 1), while Y is the odd integer with twos-complement binary representation (v_{b-2}, v_{b-4}, ... , v_0, 1). The MSBs v_{b-1} and v_{b-2} are the sign bits for X and Y respectively. Figure 7.6-5 shows example constellations for b = 2 and b= 4.

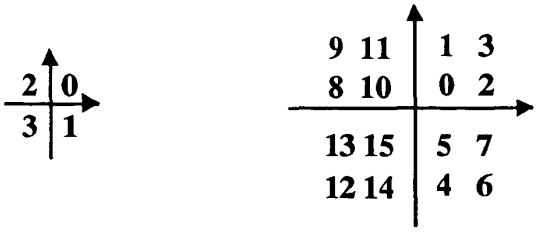

Figure 7.6-5: Constellation labels for b=2 and b=4

Note that the 4-bit constellation can be obtained from the 2-bit constellation by replacing each label n by the 2 x 2 block of labels:

4n+1	**4n+3**
4n	**4n+2**

The same procedure can be used to construct the larger even-bit constellations recursively.

The constellations obtained for even values of b are square in shape. Note that the LSBs {v_1,v_0} represent the coset labeling of the constituent 2-dimensional cosets used in the 4-dimensional Wei trellis code.

7.6.4.2 Odd values of b, b£3

Figure 7.6-6 shows the constellation for the cases b = 1 and b= 3.

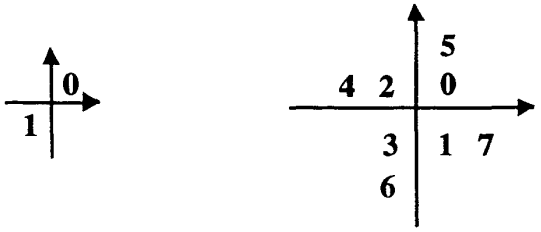

Figure 7.6-6: Constellation labels for b=1 and b=3

7.6.4.3 Odd values of b, b>3

If b is odd and larger than 3, the 2 msbs of X and the 2 msbs of Y are determined by the 5 msbs of the b bits. Let $c = (b+1)/2$, then X has twos-complement binary representation $(X_c, X_{c-1}, v_{b-4}, v_{b-6}, v_{b-8}, \ldots, v_3, v_1, 1)$, and Y has twos-complement binary representation $(Y_c, Y_{c-1}, v_{b-5}, v_{b-7}, v_{b-9}, \ldots, v_2, v_0, 1)$ where X_c and Y_c are the sign bits of X and Y respectively. The relationship between $X_c, X_{c-1}, Y_c, Y_{c-1}$ and $v_{b-1}, v_{b-2}, \ldots, v_{b-5}$ is shown in the following table.

$v_{b-1}, v_{b-2}, \ldots, v_{b-5}$	X_c, X_{c-1}	Y_c, Y_{c-1}
0 0 0 0 0	0 0	0 0
0 0 0 0 1	0 0	0 0
0 0 0 1 0	0 0	0 0
0 0 0 1 1	0 0	0 0
0 0 1 0 0	0 0	1 1
0 0 1 0 1	0 0	1 1
0 0 1 1 0	0 0	1 1
0 0 1 1 1	0 0	1 1
0 1 0 0 0	1 1	0 0
0 1 0 0 1	1 1	0 0
0 1 0 1 0	1 1	0 0
0 1 0 1 1	1 1	0 0
0 1 1 0 0	1 1	1 1
0 1 1 0 1	1 1	1 1
0 1 1 1 0	1 1	1 1
0 1 1 1 1	1 1	1 1
1 0 0 0 0	0 1	0 0
1 0 0 0 1	0 1	0 0
1 0 0 1 0	1 0	0 0
1 0 0 1 1	1 0	0 0
1 0 1 0 0	0 0	0 1
1 0 1 0 1	0 0	1 0
1 0 1 1 0	0 0	0 1
1 0 1 1 1	0 0	1 0
1 1 0 0 0	1 1	0 1
1 1 0 0 1	1 1	1 0
1 1 0 1 0	1 1	0 1
1 1 0 1 1	1 1	1 0
1 1 1 0 0	0 1	1 1
1 1 1 0 1	0 1	1 1
1 1 1 1 0	1 0	1 1
1 1 1 1 1	1 0	1 1

Table 7.6-3: Determining the top 2 bits of X and Y

Figure 7.6-7 shows the constellation for the case b = 5.

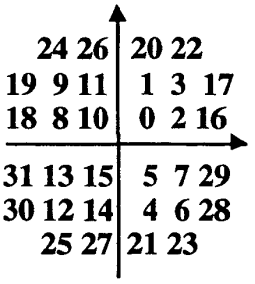

Figure 7.6-7: Constellation labels for b=5

The 7-bit constellation can be obtained from the 5-bit constellation by replacing each label n by the 2 x 2 block of labels:

4n+1	**4n+3**
4n	**4n+2**

Again, the same procedure can be used to construct the larger odd-bit constellations recursively. Note also that the LSBs $\{v_1,v_0\}$ represent the coset labeling of the constituent 2-dimensional cosets used in the 4-dimensional Wei trellis code.

***********EDITORIAL NOTE***********

Sub-clause 7.7
Status : Under Study (Oct./93 Interim Mtg.)

Source: Amati
NOTE: This sub-clause was added as a result of the concensus reached at the Oct/93 Interim meeting that the option to not provide Trellis coding should be included in the draft standard.

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7.7 Encoder (uncoded version)

An algorithmic constellation encoder is used to construct constellations with a maximum of 15 bits.

7.7.1 Bit extraction

Data bytes from the DMT symbol buffer are extracted according to a re-ordered bit allocation table b'_i, using the least-significant-bit-first convention. The number of bits per tone b'_i can take any non-negative integer values not exceeding 15, with the exception of $b'_i = 1$. For a given tone b'_i=b bits are extracted from the DMT symbol buffer. These b bits form a binary word $\{v_{b-1}, v_{b-2}, \ldots, v_1, v_0\}$.

7.7.2 Constellation encoder

The constellation encoder requirements are as specified in 7.6.4.

**********EDITORIAL NOTE**********

Sub-clause : ~~(was 7.7~~ to 7.11) is now 7.8 to 7.12
Status : Under Study (Oct./93 Interim Mtg.)
Cont. 93-193R1
Source: Amati

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7.8 Gain scaling

Each point (X_i,Y_i) or complex number $Z_i = X_i + jY_i$ output from the encoder is multiplied by the fine gain adjuster, g_i:

$$Z_i' = g_i Z_i$$

7.9 Modulation

7.9.1 Sub-carriers

7.9.1.1 Data sub-carriers

The Channel Analysis signal defined in Section 12.7 allows for a maximum of 31 carriers (at frequencies $n\Delta f$, n=1 to 31) to be used. The lower limit on n is determined by the ADSL/POTS splitting filters; if FDM is used to separate the upstream and downstream signals, the upper limit on n is set by the down/up splitting filters. The cut-off frequencies of these filters are completely at the discretion of the manufacturer because in either case the range of usable n is determined during the Channel Estimation.

7.9.1.2 Pilot [93-085]

Carrier #8 (f = 34.5 kHz) is reserved for a pilot; that is $b_8 = 0$ and $g_8 = 1$. ~~Randomization of the data on the pilot was proposed in 93-085, and will be defined after further study~~. Use of this pilot allows resolution of sample timing in a receiver modulo 8 samples. Therefore a gross timing error, which is an integer multiple of 8 samples, could still persist after a micro-interruption (e.g., a temporary short- circuit, open circuit or severe line hit); correction of these is made possible by the use of the synchronization symbol defined in Section 6.7.4.

7.9.1.3 Nyquist frequency

The carrier at the Nyquist frequency (#64) may not be used for data; other possible uses are for further study.

7.9.3 Modulation by the inverse discrete fourier transform [93-084]

The modulating transform defines the relationship between the 64 real values x_k and the Z_i'

$$x_k = \sum_{i=0}^{63} \exp(j\pi\, ki/32)\, Z_i'$$

It should be noted that the encoder and scaler generate only 31 complex values of Z_i' (plus zero at d.c. and one real value if the Nyquist frequency is used). In order to generate real values of x_k these values must be augmented so that the vector Z' has Hermitian symmetry. That is,

$$Z_i' = Z_{64-i}'^{*} \quad \text{for } i = 33 \text{ to } 63$$

7.9.4 Synchronization symbol [93-089]

The synchronization symbol permits recovery of the frame boundary after micro-interruptions that might otherwise force retraining. The characteristics of the symbol are defined here; the variation of the symbol's cyclic prefix is defined in Section 7.9.2

The symbol rate, f_{symb} = 4kHz, the carrier separation, Δf = 4.3125 kHz, and the IDFT size, N = 64, are such that a cyclic prefix of 5 samples could be used. That is,

$$(64 + 5) \times 4.0 = 64 \times 4.3125 = 276$$

The cyclic prefix, however, is shortened to 4 samples, and a synchronization symbol (with a nominal length of 68 samples) is inserted after every 68 data symbols. That is,

$$(64 + 4) \times 69 = (64 + 5) \times 68$$

The data pattern used in the synchronization symbol is the pseudo-random sequence PRU (x_n, for n = 1 to 64) defined by

$x_n = 1$ for n = 1 to 6
$x_n = x_{n-5} + x_{n-6}$ for n =7 to 64

The bits are used as follows: the first pair of bits (x_1 and x_2) is used for the d.c.and Nyquist sub-carriers (the power assigned to them is, of course, zero, so the bits are effectively ignored); then the first and second bits of subsequent pairs are used to define the X_i and Y_i. for i = 1 to 31 as follows:

x_{2i+1}, x_{2i+2}	X_i, Y_i.
0, 0	+ +
0, 1	+ -
1, 0	- +
1, 1	- -

Bits 17 and 18, which modulate the pilot carrier, are also effectively discarded because the phase of the pilot may be determined by its own random pattern (see Section 7.9.1.2)

7.10 Cyclic prefix

The cyclic prefix is used for data and synchronization symbols beginning with segment RRATES1 of the initialization sequence, as defined in Section 12.7.2.1

The last 4 samples of the output of the IDFT (x_k for k = 61 to 64) are prepended to the block of 64 samples and read out to the DAC in sequence. That is, the subscripts, k, of the DAC samples in sequence are 61...64,1...64.

7.10.1 Synchronization symbol *[93-089]*

The length of the cyclic prefix can be increased or decreased by 2 samples from its nominal 4. The method of indicating that this stuffing or robbing is going to occur is TBD.

7.11 Digital-to-analog converter

7.11.1 Conversion rate

The conversion rate shall be 276 kHz

7.11.2 Dynamic range

The maximum output signal of the DAC shall be such that the probability of the signal being clipped is no greater than 10^{-5}

7.11.3 Quantizing noise

The Signal-to-Quantizing Noise ratio (SQNR) of the DAC output is defined as the ratio of the rms value of a full-scale sine wave to the rms sum of all the non-fundamental signals generated up to half the conversion rate.

Over the frequency band 0 to 276 kHz the SQNR of the DAC shall be no less than 72 dB.

7.12 Anti-aliassing filter

The filter attenuation shall be nominally constant in a passband from 10 kHz to 138 kHz, and it shall increase at least 80 dB/decade beyond 138 kHz.

Figure 7.1-1 placed here

Figure 7.2-1 Placed here

Figure 7.2-2 Paced here

Figures 7.2-3 and 7.2-4 placed here

Figure 7.2-5 Placed here

Figure 7.2-6 Placed here

**********EDITORIAL NOTE**********

Clause 8
Status : Under Study (Oct./93 Interim Mtg.)
Cont. 93-269R1
Source: NT (Revised based on review at Oct. /93 Interim Mtg.)
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8. ADSL/POTS splitter functional characteristics

When ADSL coexists with POTS on the same line it is necessary to perform an ADSL/POTS splitting function at each end of the line.

At the U-R the splitting functions are:

1) combining the POTS and the ATU-R transmit signals towards the U-R;

2) separating the POTS and ADSL signals received from the U-R;

3) protecting the POTS from voice-band interference from signals generated by both the ATU-R and ATU-C.

4) protecting both ATU-R and ATU-C receivers from all POTS-related signals, particularly dial pulses, ringing and ring trip.

Note: Protection of the ADSL receivers from those components of POTS-related signals that fall in the voiceband may be partially performed by the receivers themselves. The amount of protection that must be performed by the splitter is *TBD*.

These functions must be performed while meeting all requirements for POTS performance, such as echo and singing return loss.

The combination/separation functions are achieved by frequency-division multiplexing (FDM). The POTS signal occupies the band up to to 3.4 kHz; the ADSL signal in the upstream direction (ATU-R to ATU-C) may occupy the band from approximately 20 to 138 kHz; the signal in the downstream direction (ATU-C to ATU-R) may occupy the band from 20 to 1104 kHz.

Note: In an FDM implementation the lower limit of the downstream band will be considerably higher than 20 kHz (it is a manufacturer's option, which will typically be about 90 kHz); this might affect the design of the splitter, but nevertheless, all functions of the splitter must be performed for the tighter, echo-cancelling, implementation.

The functional characteristics of the ADSL/POTS splitter at the ATU-C are identical to those of the splitter at the ATU-R.

9. Service module interface requirements (Under study)

9.1 AS channels

9.2 C channel

9.3 384 kbit/s full duplex

9.4 BRA ISDN

10. Electrical characteristics

**********EDITORIAL NOTE**********

Sub-clause 10.1
Status : Provisionally Agreed with changes at the Oct./93 Interim Mtg.
Cont. 93-270R1
Source: NT (Revised based on review at Oct. Mtg.)
****

10.1 Network interface (NI) requirements

10.1.1 Impedance and return loss

The nominal driving point impedance at the network interface at frequencies up to 3400 Hz, shall be 900 ohms with respect to the CO, and 600 ohms with respect to the subscriber. Over the frequency range of 138 to 1100 kHz the driving point impedance shall be 100 ohms. The return loss, looking into the ADSL/POTS splitter from the network interface, over the frequency range from 10 to 3400 Hz with respect to 600 ohms shall be greater than 20 dB when the POTS port is terminated in 600 ohms. The return loss over the frequency range of 138 to 1100 kHz, with respect to 100 ohms, shall be greater than 20 dB.

10.1.2 Longitudinal output voltage

The ATU-R shall present to the interface a longitudinal component whose rms voltage, in any 4- kHz bandwidth averaged in any 1-second period, is less than -50 dBv over the frequency range 100 Hz to 150 kHz, and less than -80 dBv over the range from 150 to 270 kHz. Compliance with this limitation is required with a longitudinal termination having an impedance equal to or greater than a 100-ohm resistor in series with a 0.15 uf capacitor.
Ground reference for these measurements shall be the building or green-wire ground of the ATU-R.

10.1.3 Longitudinal balance

The longitudinal balance (impedance to ground) is given in the following equation:

$$LBal = 20 \log \left| \frac{e_l}{e_m} \right| \text{ dB}$$

e_l = the applied longitudinal voltage (referenced to the building or green wire ground of the ATU-R);
e_m = the resultant metallic voltage appearing across a terminating resistor.

The balance shall be >60 dB at frequencies up to 3400 Hz with a terminating resistor of 600 ohms. Over the frequency range 20 to 1100 kHz, the balance shall be > 40 dB with a terminating resistor of 100 ohms.

10.1.4 Jitter TBD

10.1.5 dc characteristics TBD

10.2 Composite ADSL interface requirements TBD

10.3 POTS interface requirements TBD

11. Operations and maintenance

11.1 General ADSL system maintenance TBP

**********EDITORIAL NOTE**********

Sub-clause 11.2
Status : Provisionally Agreed (Oct./93 Interim Mtg.)
Cont. 93-253
Source: Amati

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11.2 Embedded operations channel (eoc) requirements

An embedded operations channel for communication between the ATU-C and ATU-R is used for in-service and out-of-service maintenance, for retrieval of a limited amount of ATU-R status information and ADSL performance monitoring parameters, and may also be used in the future to extend maintenance/performance monitoring to the service module(s) at the customer premises. The eoc channel is shared with user channel synchronization control of the fast data buffer. This section describes the eoc functions, protocol, and commands; insertion of eoc frames within the ADSL data frames was described in Sections 6.2 and 7.2.

11.2.1 eoc organization and protocol

The ADSL eoc is organized into eoc frames, which are transmitted within the synchronization control overhead of the fast data buffer, to allow the ATU-C (acting as master of the link) to invoke commands and the ATU-R (acting as slave) to respond to the commands.

When it is not required for synchronization control, crc, or fixed indicator bits, the "fast" byte of two successive ADSL frames, beginning with an even-numbered frame as described in Sections 6.2 and 7.2, is used to transmit one eoc frame, which consists of 13 bits. For the allowable user data configurations (see Section 5.4), up to 32 eoc frames can be transmitted per ADSL superframe, so that the eoc channel rate will vary from some minumum rate that will be dependent on the vendor's synchronization control algorithm (to implement the synchronization control described in Section 6.2) to about 23.7 kbit/s.

The eoc protocol is related to the International Standards Organization (ISO) Open Systems Interconnection (OSI) model, and is defined for Layers 1, 2, and 7 as follows.

Starting with the physical layer (OSI layer 1) specification, the ADSL eoc consists of eoc frames transmitted within the "fast byte" of the fast data buffer in two successive ADSL data frames, beginning with an even-numbered frame, whenever the "fast byte" in that even-numbered frame is not used for synchronization control, crc, or fixed indicator bits. Whenever the "fast byte" in an even-numbered ADSL frame is used for eoc, the "fast byte" in the odd-numbered frame that immediately follows is dedicated to complete the eoc frame. For the range of user data configurations currently under consideration, up to 32 eoc frames per ADSL superframe (17 msec) will be transmitted (on average) in the downstream direction (i.e., from ATU-C to ATU-R). Twenty-eight to 32 eoc frame opportunities exist per ADSL superframe in the upstream direction; however, only one eoc frame will be inserted in the upstream direction for each received eoc frame (thus the downstream direction, that is the transmission from the master node, drives the eoc rate of the ADSL link and preserves the ATU-C's status as master). *(Note: A possible exception could be made for the "dying gasp" message, which is the only autonomous message allowed from the ATU-R and is inserted as soon as upstream "fast" bytes are available).*

At the data link layer (OSI layer 2), a 13-bit eoc frame and a protocol that dictates eoc states and how frames are passed between the ATU-C and the ATU-R are defined.
The 13 bits of the eoc frame are defined in the table below; the assignment of these bits to positions within the "fast byte" was defined in Sections 6.2 and 7.2. The eoc protocol states will be defined in Sections 11.2.4.

Bit Position	#Bits	Description	Notes
1,2	2	Address	Can address 4 locations
3	1	Data ("0") or Opcode ("1")	Data used for read/write
4	1	Odd ("1") or Even ("0")	Multibyte Transmission
5	1	Unspecified (set to 1) *(see Note)*	Reserved for future use
6-13	8	Information Field	256 Opcodes, 8 bits Data

Note 1: Use of eoc5 to designate an autonomous message or an indicator message from the ATU-R that does not affect the eoc protocol state is for further study.

Because the ADSL link is point-to-point between one ATU-C unit and one ATU-R unit, the network for the eoc protocol is fixed, so that the ADSL layers corresponding to layers 3 through 6 of the OSI protocol stack are empty. The application layer (OSI layer 7) processes the ADSL eoc message set. The messages are encoded within the information field of the ADSL eoc frame, and are described in Section 11.2.3.

11.2.2 eoc frame structure

The eoc frame contains 5 fields, defined in the following sub-sections.

11.2.2.1 The Address Field

The first two bits comprise the address field and can address up to four locations, only two of which are defined at this time.

"11" ATU-C (master)
"00" ATU-R (slave)
"10" Reserved for future use
"01" Reserved for future use.

11.2.2.2 The data/opcode field

This bit indicates whether the information field of the current eoc frame contains data or an operation code for an ADSL eoc message, and is defined as follows:

"1" Information field contains an eoc message operation code
"0" Information field contains data.

11.2.2.3 "Odd byte" / "even byte" field

This bit is used in data transmission as follows. For the first byte of data to be either read or written, this bit is set to "1" to indicate "odd" byte. For the next byte, it is set to "0" to indicate "even" byte and so on, alternately. This field is used to speed up multibyte data reads and writes by eliminating the need for intermediate codes to indicate to the far end that the previous byte was successfully received.

11.2.2.4 Unspecified bit

This bit is reserved for future use and until specified otherwise, it should be set to "1". It could be used to enhance addressing for extending OAM out to the home distribution network or Service Modules, or it could be used to allow autonomous messages from the ATU-R without disturbing the current state of the eoc protocol.

11.2.2.5 Information field

Up to 256 different messages or 8 bits of binary or ASCII data may be encoded in the Information Field.

Note: The message set is restricted to codes that provide a minimum Hamming distance of 2 between all opcodes, and a minimum distance of 3 between certain critical codes and all other codes.

11.2.3 eoc message sets

The ATU-C, as the master, sends commands to the ATU-R, as slave, to perform certain functions. Some of these functions require the ATU-R to activate changes in the circuitry (e.g., to send crc bits that are corrupt). Other functions that can be invoked are to read from and write into data registers located at the ATU-R. The data registers are used for reading status or performance monitoring parameters from the ATU-R, or for limited maintenance extensions to the customer premises wiring distrubution network or Service Modules.

Some of these commands are "latching", meaning that a subsequent command will be required to release the ATU-R from that state. Thus multiple ADSL eoc-initiated actions can be in effect simultaneously. A separate command, "Return To Normal", is used to unlatch all latched states. This comand is also used for bringing the network to a known state, the idle state, when no commands are active in the ATU-R location. On the other hand, to maintain the latched state, the command "Hold State" has to be continually sent.

The ATU-C is the master of the ADSL eoc and always issues the commands. The ATU-R, the slave node, responds by acknowledging to the master that the message was received correctly. Thus, the ADSL eoc protocol operates in a Command/Response mode with the master issuing the command and the slave responding.

11.2.3.1 eoc message set requirements

The actions taken by the ATU-R and ATU-C in response to correctly received messages are

1. *Hold State*: This message is sent by the ATU-C to the ATU-R to maintain the ATU-R eoc processor and any active ADSL eoc-controlled operations (such as latching commands) in their present state.

2. *Return to Normal (Idle Code)*: This message releases all outstanding eoc-controlled operations (latched conditions) at the ATU-R and returns the ADSL eoc processor to its initial state. This code is also the message sent during idle states.

3. *Unable to Comply Acknowledgement*: The ATU-R shall send this message when it receives an ADSL eoc message (three times consecutively and identically) that the ATU-R cannot perform, either because it does not recognize or implement the command, or because the command is unexpected* given the current state of the ADSL eoc interface.

   *(*Examples:*

   (a) the command indicates that the information field contains data, but the command was not preceded by a "Write Data" command;

   (b) the command requests the "Next Byte" in Data Read mode after all bytes have been read from the specified register).

4. *Request Corrupt crc*: This message requests the ATU-R to send corrupt crcs toward the ATU-C until canceled with the "Request End of Corrupt crc" or "Return to Normal" message.

   The "Request corrupt crc" command shall be latching, permitting multiple ADSL eoc-initiated actions to be in effect simultaneously.

5. *Request End of Corrupt crc*: This message requests the ATU-R to stop sending corrupt crcs toward the ATU-C.

6. *Notify of Corrupted crc*: This message notifies the ATU-R that intentionally corrupted crcs will be sent from the ATU-C until cancellation is indicated by "Notify End of Corrupted crc" or "Return to Normal".

7. *Notify End of Corrupted crc*: This message notifies the ATU-R that the ATU-C has stopped sending corrupted crcs.

8. *Perform Self Test*: This message requests the ATU-R to perform a self test. The result of the self test is stored in a register at the ATU-R (After the self test, the ATU-C re-establishes the link and reads the test results from the ATU-R register).

9. *Write Data (Register #)*: This message directs the ATU-R to enter the Data Write Protocol state to receive data in the register specified by the Opcode.

10. *Read Data (Register #)*: This message directs the ATU-R to enter the Data Read Protocol state to transmit data to the ATU-C from the register specified by the Opcode.

11. *Next Byte*: This message is sent by the ATU-C in Data Read or Data Write mode after the ATU-R has acknowledged the previously sent Read or Write Data command. This message is continually sent by the ATU-C when it is in the Data Read or Data Write mode, toggling bit four for multi-byte data, until all data has been read.

12. *End of Data*: This message is sent by the ATU-C after it has written all bytes of data to the ATU-R. This message is also sent by the ATU-R in response to a "Next Byte" message from the ATU-C that is received after all bytes have been read or written from the currently addressed ATU-R register.

13. *Vendor Proprietary Opcodes*: Four opcodes have been reserved for vendor proprietary use. The ATU-C must read the CLEI (Common Language Equipment Identifier) register of the ATU-R to ensure compatibility between the ATUs before using proprietary opcodes.

14. *Undefined Command Codes*: All command codes not defined are reserved for future use, and shall not be used for any purpose.

11.2.3.2 eoc opcode messages

(HEX)	Opcode Meaning	Notes
01	Hold State	To continue sending corrupt crcs
F0	Return to normal all active conditions	Also used as "idle code"
02	Perform "Self Test"	Self test results are stored in register
04	Unable to Comply (UTC)	Unrecognizable command
07	Request Corrupt crc*	
08	Request end of Corrupt crc	
0B	Notify Corrupt crc*	
0D	Notify end of Corrupt crc	
0E	End of Data	
10	Next Byte	
(20,23,25,26) (29,2A,2C,2F) (31,32,34,37) (38,3B,3D,3E)	Write data Register Nos. 0 thru F	
(40,43,45,46) (49,4A,4C,4F) (51,52,54,57) (58,5B,5D,5E)	Read data Register Nos. 0 thru F	
(19,1A,1C,1F)	Vendor proprietary protocols	

* latching conditions

The eoc opcode messages specified in the above table guarantee a minimum Hamming distance of 2 (by requiring odd parity) between all opcodes, and a minimum Hamming distance of 3 between the "Return to Normal" (or "idle") code and all other codes.

The following codes, which still maintain a minimum Hamming distance of 2, should not be used (unless specified at some future time):

(hexidecimal) 13, 15, 16,
80, 83, 85, 86, 89, 8A, 8C, 8F.

An additional code, which would maintain a minimum Hamming distance of 3 with all above codes (including the "Return to Normal" or "idle" code), is E7. *(Note: This code could be used to implement a "dying gasp" autonomous message).*

11.2.3.3 Data registers in the ATU-R

REG # (HEX)	USE	LENGTH	DESCRIPTION
0	TBD	TBD	TBD
1	R	TBD	CLEI code (ATU-R)
2	R	TBD	Serial #
3	R	1 byte	Self Test Results
4	R/W	Vendor Defined	Vendor Defined
5	R/W	Vendor Defined	Vendor Defined
6	R	1 byte	Signal Power (-60 dBm to +30 dBm)
7	R	1 byte (TBR)	Estimated Margin (TBR)
8	R	18	ATU-R Configuration*: one byte each for $B_F(AS0)$, $B_I(AS0)$, $B_F(AS1)$,$B_I(AS1)$, $B_F(AS2)$, $B_I(AS2)$, $B_F(AS3)$, $B_I(AS3)$, $B_F(LS0)$, $B_I(LS0)$, $B_F(LS1)$, $B_I(LS1)$, $B_F(LS2)$, $B_I(LS2)$, P_{dsf}, P_{dsi}, P_{usf}, P_{usi}
9	R/W	TBD	Service Module Maintenance Control** (includes any writable OAM parameters or commands)
A	R	TBD	Service Module Status** (includes any OAM parameters or indicators)
B - F	TBD	TBD	TBD

* ATU Configuration Parameter set ($B_F(\ )$, $B_I(\ )$, P_{dsf}, P_{dsi}, P_{usf}, P_{usi}) defined in Sections 6.2 and 7.2.

** These ATU-R registers are included to allow future extension of maintenance to Service Modules or a customer premises wiring distribution network. The type of interface provided from these registers to customer premises equipment and the protocol for their use are topics left for further study.

11.2.4 eoc protocol states

The ADSL eoc protocol operates in a repetitive command/response mode. The ATU-C acts as the master and issues commands; the ATU-R acts as slave and responds to the commands issued by the ATU-C. Three identical properly-addressed consecutive messages shall be received before an action is initiated. Only one message, under the control of the ATU-C, shall be outstanding (not yet acknowledged) on the ADSL eoc at any one time.

Three types of responses are allowed from the slave; thus there are three command / response protocol states allowed on the ADSL eoc. The three states are

1. Message / Echo-response protocol state.
2. Message / Unable-to-Comply-response protocol state.
3. Message / Data-response protocol state.

Note: In addition to these three states, one autonomous message set could be allowed from the ATU-R to the ATU-C to indicate "dying gasp". This message does not change the protocol state; however, other actions (e.g., an automatic reset at the ATU-C) taken as a result of receiving this message may lead to a change of state (e.g., back to idle). This issue is for further study.

The ATU-C shall continuously send an appropriately addressed message. In order to cause the desired action in the addressed element, the ATU-C shall continue to send the message until it receives three identical consecutive eoc frames from the addressed device. The command / response protocol for that message must be completed before a new message (which may induce a different protocol state in the slave) may be issued.

11.2.4.1 Message / echo-response protocol state

To initiate an action at the ATU-R, the ATU-C shall begin sending eoc messages with the Data/Opcode set to "0" and with the appropriate message opcode in the information field.

The ATU-R shall initiate action when, and only when, three identical, consecutive, and properly addressed eoc frames, which contain a message recognized by the ATU-R, have been received. The ATU-R shall respond to all received messages. The response shall be an echo of the received ADSL eoc message. The combination of the master sending an ADSL eoc frame and the slave node echoing the frame back comprises the message / echo-response protocol state.

For the master node to confirm correct reception of the message by the slave node, the message / echo-response ADSL eoc protocol state is repeated until the master node receives three identical and consecutive echoes. This serves as an implicit acknowledgment to the master that the slave has correctly received the transmitted message and is acting on it. This completes the Message / Echo-response protocol mode.

Under error-free conditions, the master starts receiving the first echo from the slave only when it is preparing to repeat the frame for the third time; the third consecutive echo will be received when the master is preparing to repeat the frame for the fifth time. Thus it takes five eoc frames to complete a message; since eoc frames are inserted into ADSL frames only when the "fast byte" is available, the amount of time it will take to complete a message under error-free conditions will depend on the vendor's synchronization control algorithm.

The ATU-C continuously sends the activating message after the receipt of the three valid echoes, or alternatively, it may switch to sending the Hold State message. If the message was one of the latching commands, then the ATU-R will maintain the commanded condition until the ATU-C issues the appropriate command that ends the specific latched condition or until the ATU-C issues the Return to Normal command (at which time all latched conditions in the ATU-R must be terminated).

11.2.4.2 Message / unable-to-comply response protocol state

When the slave node (ATU-R) does not support a message that it has received three times identically and consecutively, the slave responds with the Unable-To-Comply ADSL eoc response mesage with its own address in lieu of a third identical and consecutive echo. In this manner the slave will switch to the message / UTC-response protocol state.

When the ATU-C is trying to activate an eoc function, autonomous messages from the ATU-R will interfere with confirmation of receipt of a valid eoc message. The sending by the ATU-R and receipt by the ATU-C of three identical consecutive properly addressed Unable-to-Comply messages constitutes notification to the ATU-C that the ATU-R does not support the requested function, at which time the ATU-C may abandon its attempt.

11.2.4.3. Message / data-response protocol state

The master can either write data into the slave memory, or read data from the slave memory.

11.2.4.3.1 Data read protocol

To read data from the slave, the master will send an appropriate read opcode message to the slave that specifies the register to be read. After receiving three identical and consecutive acknowledgments, the master will request the first byte to be sent from the slave by sending "Next Byte" messages with bit four set to "1", indicating a request for an "odd" byte. The slave will respond to these "Next Byte" messages by echoing them until it has received three such messages consecutively and identically. Beginning with the third such reception, the slave will respond by sending the first byte of the register in the information field of an ADSL eoc frame with bit four set to "1" to indicate "odd byte" and with bit 3 set to "0" to indicate that the eoc frame is a data frame (as opposed to a frame that contains an opcode in the information field). The master continues to send the "Next Byte" message with bit four set to "odd byte", and the slave continues to respond with a data frame containing the first byte of data and bit four equal to "odd byte", until the master has received three consecutive and identical data frames with bit four set to "odd byte".

If there is more data to be read, the master requests the second byte of data by sending "Next Byte" messages with bit four set to "0" ("even byte"). The slave echoes all messages received until three such "Next Byte" messages have been received, and on the third consecutive and identical "Next Byte" message, the slave starts sending data frames containing the second byte of the register with bit four set to "0". The master continues to send the "Next Byte"

message with bit four set to "even byte", and the slave continues to respond with a data frame containing the identical data frames with bit four set to "even byte".

The process continues for the third and all subsequent bytes with the value of bit four toggling from "odd byte" to "even byte" or vice versa, on each succeeding byte. Each time bit four is toggled, the slave echoes for two correct frames, and starts sending the data frame on the third reception. The process ends only when all data in the register has been read.

Once the slave is in the Data Read mode, to continue reading data, the only message that the master is allowed to send is the "Next Byte" message with bit four toggling. To end the Data Read mode abnormally, the master sends either "Hold State" or "Return to Normal", depending on whether any latched states are to be retained. If the slave receives any other message three times consecutively and identically while it is in Data Read mode, the slave goes into a UTC mode.

If, after all bytes have been read from the ATU-R register, the master continues to send the "Next Byte" message with bit four toggled, then the slave will send an "End of Data" message (with bit three set to "1" indicating opcode).

The Data Read mode ends either when the master has received the last requested data byte three times consecutively and identically or when the master has received three "End of Data" messages with bit three set to "1" consecutively and identically. The master then switches over to a known state with the "Hold State" or "Return to Normal" message, and the ATU-R releases the register and ends the Data Read mode.

11.2.4.3.2 Data write protocol

To write data to the slave's memory, the master will send a "Write Data" opcode message to the slave that specifies the register to write into. When the slave acknowledges with an echo message, three times identically and consecutively, the master sends the first byte of data. The slave will acknowledge the receipt of the byte with an echo of the message. After the master is satisfied with three identical and consecutive correct echo responses, it starts sending the next byte of data. Each time the master receives three identical and consecutive correct data echo responses, it will switch to sending the next byte of data. It will also toggle the "odd/even" bit accordingly. ("Next Byte" messages are not used in the Data Write mode). The master will end the write mode with the "End of Data" message indicating to the ATU-R to release the register and end the data write mode.

11.2.4.2 "dying gasp"

Note: *This issue is for further study. A possible implementation of the "dying gasp" follows:*

When circuits in the ATU-R detect that electrical power has been shut off, the ATU-R will insert eoc frames into the ADSL upstream to implement a "dying gasp". The "dying gasp" eoc frames will have bit 5 set to "0" to indicate autonomous message, bit 3 set to "1" to indicate opcode, and will contain the "dying gasp" opcode (hexadecimal E7, which has a minimum Hamming distance of 3 to all other opcodes) in the info field. At least six of these frames are inserted in the next (twelve) available ADSL upstream "fast" bytes, regardless of the number of eoc frames received in the downstream.

***********EDITORIAL NOTE***********

Sub-clause 11.3 to 11.3.2
Status : Provisionally Agreed (Oct./93 Interim Mtg.)
Cont. 93-175
Source: Amati and NT

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11.3 In-service performance monitoring and surveillance

With reference to Fig. 11.1, the following terminology is used in this standard:

Near-end means performance of the loop-side received signal at the input of the ATU-C, and at the input of the ATU-R.

Far-end means performance of the loop-side received signal at the input of the ATU-R, as reported to the ATU-C in overhead indicators. (Far-end also means performance of the loop-side received signal at the input of the ATU-C, as reported to the ATU-R in overhead indicators. This case is essentially a mirror image of the above, and is not specifically addressed in this standard.

In addition, the following terminology applies:

Primitives are basic measures of performance, usually obtained from digital signal line codes and frame formats, or as reported in overhead indicators from the far-end. Performance primitives are categorized as events, anomalies and defects. Primitives may also be basic measures of other quantities (e.g., AC power), usually obtained from equipment indicators.

Events are bit error related primitives that do not affect service performance (fec and fecc).

Anomalies are bit error related primitives that affect service performance (crc and febe).

Defects are signal or framing related primitives that are more disruptive to service than anomalies (los, sef, rdi).

According to the precedent set in other DSL related ANSI documents (e.g., ISDN BRA, HDSL), acronyms for primitives are written in lower case.

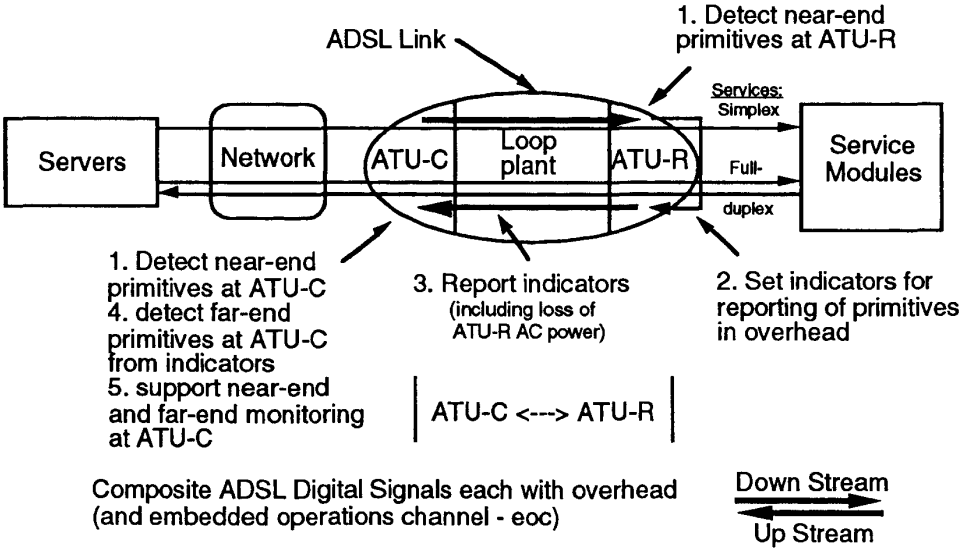

Figure 11.1 - In-service surveillance of the ADSL link

11.3.1 Digital transmission related primitives

11.3.1.1 Near-end events

Forward error correction (fec)-i
A fec-i event occurs when a received FEC code for the interleaved (i) data stream indicates that errors have been corrected.

Forward error correction (fec)-ni
A fec-ni event occurs when a received FEC code for the non-interleaved (ni) data stream indicates that errors have been corrected.

11.3.1.2 Far-end events (ATU-R is at the far-end)

Forward error correction count (fecc)-i
fec-i is reported by the fecc-i indicator.* A fecc-i event occurs when a received fecc-i indicator is set to '0' for the interleaved data stream.

Forward error correction count (fecc)-ni
fec-ni is reported by the fecc-ni indicator.* A fecc-ni event occurs when a received fecc-ni indicator is set to '0' for the non-interleaved data stream.

* The fecc-i and fecc-ni indicators are each coded with one indicator bit in the ATU-R to ATU-C overhead, and are reported once per ADSL superframe. For each bit, '1' means no event is present , and '0' means an event is present, in the previous superframe.

11.3.1.3 Near-end anomalies

Cyclical redundancy check (crc)-8i error
A crc-8i anomaly occurs when a received CRC-8 code for the interleaved (i) data stream is not identical to the corresponding locally generated code.

Cyclical redundancy check (crc)-8ni error
A crc-8ni anomaly occurs when a received CRC-8 code for the non-interleaved (ni) data stream is not identical to the corresponding locally generated code.

11.3.1.4 Far-end anomalies (ATU-R is at the far-end)

Far-end block error count (febe)-i
crc-8i is reported by the febe-i indicator.* A febe-i anomaly occurs when a received febe-i indicator is set to '0' for the interleaved data stream.

Far-end block error count (febe)-ni
crc-8ni is reported by the febe-ni indicator.* A febe-ni anomaly occurs when a received febe-ni indicator is set to '0' for the non-interleaved data stream.

* The febe-i and febe-ni indicators are each coded with one indicator bit in the ATU-R to ATU-C overhead, and are reported once per ADSL superframe. For each bit, '1' means no anomaly is present, and '0' means an anomaly is present, in the previous superframe.

11.3.1.5 Near-end defects

Loss-of-signal (los)
A los defect occurs when received ADSL pilot tone power, averaged over a 0.1 sec. period, is 6 or more dB below the pilot tone reference power, the reference power being that averaged for 0.1 sec. after the start of steady state data transmission (i.e., after initialization). A los defect terminates when the received ADSL pilot tone power, averaged over a 0.1 sec. period, is less than 6 dB below its reference power.

Severely errored frame (sef)
A sef defect occurs when the content of two consecutively received ADSL synchronization symbols does not match the expected content. An sef defect terminates when the content of two consecutively received ADSL synchronization symbols matches the expected content.

11.3.1.6 Far-end defects (ATU-R is at the far-end)

Loss-of-signal (los)
A los defect as detected at the far-end is reported by the los indicator.# A far-end los defect occurs when 4 or more out of 6 contiguously received los indicators are set to '0'. A far-end los defect terminates when 4 or more out of 6 contiguously received los indicators are set to '1'.

The los indicator is coded with one indicator bit in the ATU-R to ATU-C overhead, and is reported every ADSL superframe for 0. 1 sec. (i.e., for 5 or 6 contiguous superframes). For each bit, '1' means no defect is being reported, and '0' means a defect is being reported.

Remote Defect Indication (rdi)
An sef defect is reported by the rdi signal.* A rdi defect occurs when a received rdi signal is set to '0'. A rdi defect terminates when a received rdi signals is set to '1'.

* The rdi signal is coded with one indicator bit in the ATU-R to ATU-C overhead, and is reported once per ADSL superframe. For each bit, '1' means no defect is present, and '0' means a defect is present, in the previous superframe.

11.3.2 Other Primitives

11.3.2.1 Other near-end primitives

Signal power (sp)
A sp primitive is the sum of all received active DMT subcarrier powers at the input of the ATU, averaged over a 1 sec. period. The sp primitive is expressed as an integer number of dBm (where 0 dBm is 1 milliWatt into 100 Ohms), and ranging from a min. of -60 to a max. of +30 dBm.

Loss-of-power (lopr)
A lopr primitive occurs when ATU AC power drops to a level equal to or below the manufacturer determined minimum power level required to ensure proper operation of the ATU. A lopr primitive terminates when the power level exceeds the manufacturer determined minimum power level.

11.3.2.2 Other far-end primitives (ATU-R is at the Far-End)

Signal power (sp)
A sp primitive as detected at the far-end is reported by the sp indicator.# A far-end sp primitive occurs when one sp indicator is received with value not less than -60 and not more than +30 dBm.

The sp primitive is stored in a 8 bit register for nominally 1 sec. in the ATU-R. The sp indicator is reported once per second in an ATU-R to ATU-C eoc message, in response to once per second read requests from the ATU-C.

Loss-of-power (lopr)
A lopr primitive as detected at the far-end is reported by the lopr indicator.* A far-end lopr primitive occurs when 4 contiguous lopr indicators are received. A far-end lopr primitive terminates if the near signal remains present, i.e., if the received 4 contiguous lopr indicators are not followed by any near-end los defects in the next 0.5 sec. (see los defect definition in 11.3.1.5).

* The lopr indicator is coded as an 8 bit emergency priority message in the ATU-R to ATU-C overhead, and is reported in x contiguous frames that support the emergency priority message. The value of x, and the message structure is under study.

**********EDITORIAL NOTE**********

Sub-clause 11.3.3 to 11.3.5
Status : Under Study (Oct./93 Interim Mtg.)
Cont. 93-213
Source: NT
NOTE:
This strawman text was forwarded to T1M1.3 with a request for them to provide the required text for these topics given this area is their responsibility. The final text for 11.3.3 to 11.3.5 will be dependent on what T1M1.3 recommends.

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11.3.3 Parameters

11.3.3.1 Near-end parameters

Errored Second (ES)
ES is a count of one-second intervals containing one or more crc-i or crc-ni anomalies, or one or more los or sef defects.

Forward Error Correction (FEC)
FEC is a count of fec-i plus fec-ni anomalies.

Severely Errored Frame Second (SEFS)
SEFS is a count of one-second intervals containing one or more sef defects.

Minimum Signal Power (MSP)
MSP is the minimum of all sp primitives.

11.3.3.2 Far-end parameters (ATU-R is at the far-end)

Errored Second (ES)ES is a count of one-second intervals containing one or more febe-i or febe-ni anomalies, or one or more far-end los or rdi defects.

Forward Error Correction (FEC)
FEC is a count of fecc-i plus fecc-ni anomalies.

Severely Errored Frame Second (SEFS)
SEFS is a count of one-second intervals containing one or more rdi defects.

Minimum Signal Power (MSP)
MSP is the minimum of all far-end sp primitives.

11.3.4 Failures

11.3.4.1 Near-end failures

Loss-of-Signal (LOS)
A LOS failure is declared after 2.5 ± .5 seconds of contiguous los defect, and cleared after 10 ± .5 seconds of no los defect.

Loss-of-Frame (LOF)
A LOF failure is declared after 2.5 ± .5 seconds of contiguous sef defect, and cleared after 10 ± .5 seconds of no sef defect.

Loss-of-Power (LOPr)
A LOPr failure is declared after the occurrence of a lopr primitive which persists for 2.5 ± .5 seconds. A LOPr failure is cleared after 10 ± .5 seconds of no lopr primitive.

11.3.4.2 Far-end failures (ATU-R is at the far-end)

Loss-of-Signal (LOS)
A far-end LOS failure is declared after 2.5 ± .5 seconds of contiguous far-end los defect, and cleared after 10 ± .5 seconds of no far-end los defect.

Remote Failure Indication (RFI)
A RFI is declared after 2.5 ± .5 seconds of contiguous rdi defect, and cleared after 10 ± .5 seconds of no rdi defect.

Loss-of-Power (LOPr)
A LOPr failure is declared after receiving a far-end lopr primitive, and after 2.5 ± .5 seconds of contiguous near-end los defect. A LOPr failure is cleared after 10 ± .5 seconds of no near-end los defect.

11.3.5 Performance Monitoring Functions

11.3.5.1 Performance data storage

A current 15 min. and a current 1 day register shall be provided for each near-end and for each far-end parameter. x previous 15 min. and one previous 1 day register shall be provided for each near-end and for each far-end parameter. The value of x is understudy.

Register sizes shall accommodate maximum event counts or values in 15 min. and 1 day intervals, or have a size of at least 16 bits. Register operation shall comply with clause 9 of dpANSI T1.231-1993 on "In-Service Layer 1 Digital Transmission Performance Monitoring".

11.3.5.2 Performance data thresholding and alerting

A current 15 min. and a current 1 day threshold shall be provided for each of the near-end and far-end ES and FEC parameters (total of 8 threshold mechanisms). Thresholding for other parameters is optional. Thresholding and alerting operation shall comply with clause 9 of dpANSI T1.231-1993 on "In-Service Layer 1 Digital Transmission Performance Monitoring".

11.3.5.3 Performance data reporting

Performance data shall be reportable on demand when queried by an operations entity. Reporting details shall comply with clause 9 of dpANSI T1.231-1993 on "In-Service Layer 1 Digital Transmission Performance Monitoring".

12. Initialization

**********EDITORIAL NOTE**********

Clause 12
Status: Provisionally Agreed (Oct./93 Interim Mtg.)
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12.1 Overview

ATU-C	ACTIVATION (12.2)	TRANSCEIVER TRAINING (12.4)	CHANNEL ANALYSIS (12.6)	EXCHANGE (12.8)
ATU-R	ACKNOW-LEDGMENT (12.3)	TRANSCEIVER TRAINING (12.5)	CHANNEL ANALYSIS (12.7)	EXCHANGE (12.9)

Figure 12.1.1 Overview of Initialization

12.1.1. Basic functions of initialization

ADSL transceiver initialization is required in order for a connected ATU-R and ATU-C pair to establish a communications link. In order to maximize the throughput and/or reliability of this link, ADSL transceivers must determine certain relevant attributes of the connecting channel, and establish transmission and processing characteristics suitable to that channel. The time line of Figure 12.1.1 provides an overview of this process. In Figure 12.1.1, each receiver can determine the relevant attributes of the channel through the transceiver training and channel analysis procedures. Certain processing and transmission characteristics can also be established at each receiver during this time. During the exchange process each receiver shares with its corresponding far-end transceiver certain transmission settings that it expects to see. Specifically, during exchange each receiver communicates to its far-end transceiver the number of bits and relative power levels to be used in each DMT sub-carrier bin, as well as any messages and final data rates information. For highest performance these settings will be based on the results obtained through the transceiver training and channel analysis procedures.

Determination of channel attribute values and establishment of transmission characteristics requires that each transceiver produce, and appropriately respond to, a specific set of precisely-timed signals. This section describes these initialization signals, along with the rules that determine the proper starting and ending time for each signal. This description is made through the definition of initialization signaling states, in which each transceiver will reside, and initialization signals, which each transceiver will generate.

At any given time while a transceiver is initializing, the transceiver will reside in one of several uniquely named signaling states. The signal that the transceiver is to generate at any time during initialization is specified by the signaling state in which the transceiver presently resides. A signaling state and the signal generated while residing in that state are both given the same name. During a successful initialization procedure, the sequence of generated downstream and upstream signals is shown by the time-line of Figure 12.1.2 through Figure 12.1.5. The dashed

arrow indicates that the change of state is due to a successful reception of a specific signal. For example, in Figure 12.1.4, ATU-R stays in state R-REVERB3 until it finishes receiving C-CRC2, at which point, ATU-R moves on to R-SEGUE2 after appropriate delay (see Secction 12.7.2).

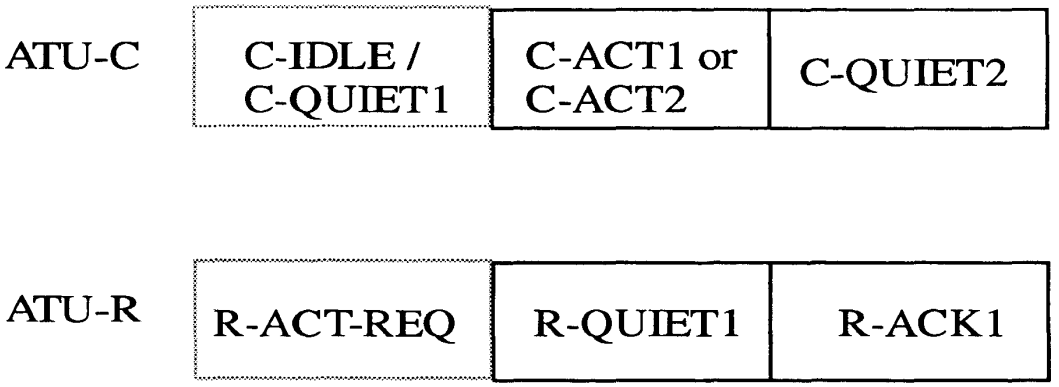
The description of a signal will consist of three components. The first component is a description of the voltage waveform that the transceiver must produce at its output during the corresponding signaling state. The second is a statement of the length of time, expressed in DMT symbol periods, during which that signal is to be generated. This signal duration, denoted $L_{SIGNALNAME}$ for a signal named SIGNALNAME, may be a constant, or may depend upon the detected signaling state of the far end transceiver. The third component of a signal's description is a statement of the rule governing which signaling state is to be entered next.

With respect to the second component above, note that the length of time spanned by a single symbol period depends on whether the cyclic prefix is being used; some initialization signals contain a cyclic prefix, and some do not. ATU-C signals up to and including C-SEGUE1 are transmitted without a cyclic prefix; those from C-RATES1 on are transmitted with a prefix. Similarly, ATU-R signals up to and including R-SEGUE1 do not use a prefix; those from R-REVERB3 on do. The duration of any signal is defined as a number of symbol periods, with the periods being of the length in effect during the transmission of that symbol.

The output voltage waveform of a given initialization signal is described through the DMT transmitter reference model shown in Figure 12.1.6. Figure 12.1.6 is not a requirement or suggestion for building a DMT transmitter. Rather, it is a model for facilitating accurate and concise DMT signal waveform descriptions. In Figure 12.1.6, N is the length of the Inverse Discrete Fourier Transform (IDFT), ν is the cyclic prefix length, X_k^n is DMT sub-carrier k during symbol period n, and x_k^n is the k'th D/A input sample during symbol period n. The details concerning these parameters are given in Figure 12.1.6. The D/A & Analog Processing block of Figure 12.1.6 construct the continuous transmit voltage waveform corresponding to the discrete D/A input samples. More precise specifications for this analog block arise indirectly from the analog transmit signal linearity and power spectral density specifications of Section 10.1. The use of Figure 12.1.6 as a transmitter reference model allows all initialization signal waveforms to be described through the sub-carrier sequence X_k^n required to produce that signal. Allowable differences in the characteristics of different D/A & Analog Processing blocks will produce somewhat different continuous-time voltage waveforms for the same initialization signal. However, a compliant transceiver will produce initialization signals whose underlying DMT sub-carrier sequences match exactly those provided in the signal descriptions of Sections 12.2-12.9.

12.1.2. Transparency to methods of separating upstream and downstream signals.

Manufacturers may choose to implement this standard using either Frequency-Division-Multiplexing (FDM) or Echo Canceling (EC) to separate upstream and downstream signals. The initialization procedure described in this section ensures compatibility between these different implementations. This is done by specifying all upstream and downstream control signals to be in the appropriate, but narrower, frequency bands that would be used by an FDM transceiver, and by defining a time period during which an EC transceiver may train its echo canceler.



(Drawn Not to Scale)

Figure 12.1.2 Timing Diagram of Activation and Acknowledgment (12.2-12.3)

12.2. Activation (ATU-C)

A host controller may be used to moniter the ATU-C activities. There are various points at the initialization sequence that detects some kind of errors, malfunction, or problems, and needs to come back to the initial state C-ACT1 (or C-ACT2) for retraining. In addition, after we have successfully gone through initialization and on to steady-state data transmission, these are cases where it may be necessary to perform a retraining. The ATU-C controller should be able to keep track of which state the error is originated from when ATU-C enters C-ACT1 (or C-ACT2) or C-IDLE/C-QUIET1. An example of an overall state diagram is shown in Annex A.

12.2.1. C-IDLE/C-QUIET1

Upon power-up, ATU-C may go through self-test. In any case, ATU-C enters the either state C-IDLE or C-QUIET1, both of which is a silent signal given by

$$C-IDLE = C-QUIET1 = X_k^n = X_k = \{0, 0 \le k \le 256$$

The difference between C-IDLE and C-QUIET1 is that the ATU-C receiver is shut off at state C-IDLE whereas the ATU-C receiver is active at state C-QUIET1. C-IDLE is transmitted indefinitely until, for instance, it receives a command from the host controller (see Annex A). In that case, the ATU-C goes to C-ACT1 (or C-ACT2, see section 12.2.2). If the ATU-C is at C-QUIET1, then another command from the host controller could trigger the ATU-C to enter C-ACT1 or C-ACT2. Alternatively, when ATU-C is at state C-QUIET1, a successful detection of R-ACT-REQ propels ATU-C to enter C-ACT1 (or C-ACT2). Since R-ACT-REQ consists of 128 symbols (Section 12.3.1), and to allow for full compatibility between FDM and EC systems, we require that regardless of how many received symbols the ATU-C receiver needs to measure before declaring a successful detection of R-ACT-REQ, the ATU-C is held silent (in C-QUIET1 state) until the ATU-C receiver ceases to detect the presence of R-ACT-REQ signal, at that time ATU-C enters C-ACT1 (or C-ACT2).

12.2.2. C-Activate

To allow for inter-operability between FDM and EC systems, and among different vendors with different implementation of such systems, we allocate two activate signals to distinguish different system requirements. The two activate signals are called C-ACT1 and C-ACT2, as described later in this section. These two signals are mutually exclusive, meaning that any given ATU-C will transmit one and only one of these two activate signals.

For any ATU-C that performs loop-timing (locking the DAC clock and the ADC clock at the ATU-C together) and slaves the ATU-C ADC clock to the DAC clock at the ATU-R, C-ACT1 is sent. Otherwise, C-ACT2 is transmitted.

12.2.2.1. C-ACT1

C-ACT1 at ATU-C is transmitted to initiate a communication link to ATU-R, when the ATU-C performs received clock slaving and loop-timing (slaving the received ADC clock at the ATU-C to the DAC clock at the ATU-R, and slaving the transmitted DAC clock to the received ADC clock). C-ACT1 consists of a single frequency sinusoid at $f_{C\text{-}ACT1}$ = 207 kHz.

Using Figure 12.1.6 as the reference model, C-ACT1 is given by

$$X_k^n = X_k = \begin{cases} 0, k \neq 48, 0 \leq k \leq 256 \\ A_{C-ACT1}, k = 48 \end{cases}$$

where $A_{C\text{-}ACT1}$ is an appropriate level so that the transmit power level is at -4 dBm (approximately -40 dBm/Hz over 4.3125 KHz) for the first 64 symbols, and at -28 dBm for the second 64 symbols. This signal is transmitted for $L_{C\text{-}ACT1}$ = 128 consecutive symbols, and no cyclic prefix is used. C-QUIET2 follows immediately after C-ACT1.

12.2.2.2. C-ACT2

C-ACT2 at ATU-C is transmitted to initiate a communication link to ATU-R, when the ATU-C does **not** guarantee performing received clock slaving and loop-timing (slaving the received ADC clock at the ATU-C to the DAC clock at the ATU-R, and slaving the transmitted DAC clock to the received ADC clock). C-ACT2 consists of a single frequency sinusoid at $f_{C\text{-}ACT2}$ = 189.75 kHz. Referring to Figure 12.1.6, C-ACT2 is given by

$$X_k^n = X_k = \begin{cases} 0, k \neq 44, 0 \leq k \leq 256 \\ A_{C-ACT2}, k = 44 \end{cases}$$

$L_{C\text{-}ACT2}$ is also equal to 128 consecutive symbols with no cyclic prefix, with transmit power level equal to -4 dBm for the first 64 symbols and -28 dBm for the second 64 symbols. Similar to C-ACT1, C-QUIET2 follows immediately after C-ACT2.

12.2.3. C-QUIET2

Immediately following C-ACT1 or C-ACT2 is C-QUIET2, a silent signal given by

$$C-QUIET2 = X_k^n = X_k = \{0, 0 \leq k \leq 256$$

C-QUIET2 is transmitted for $L_{C\text{-}QUIET2}$ = 128 consecutive symbols without cyclic prefix. The purpose of C-QUIET2 is to allow the detection of R-ACK1 without the need to train the ATU-C echo canceller.

Upon completion of C-QUIET2, ATU-C enters one of three states: (1) C-ACT1 (or C-ACT2, depending on which C-Activate signal was sent before) if the receiver at ATU-C fails to detect the presence of R-ACK1 at $f_{R\text{-}ACK1}$ = 25.875 KHz (see Section 12.3.2), and the state C-ACT1 (or C-ACT2) has not been revisited for more than twice. (There is a counter keeping track of how many times ATU-C goes from C-QUIET2 back to C-ACT1 (or C-ACT2), this counter is reset upon entering C-QUIET1), (2) C-QUIET1 if we fail to detect C-ACK1 after returning to C-ACT1 (or C-ACT2) two times, (3) C-REVEILLE if the receiver at ATU-C detects R-ACK1.

ATU-C enters C-REVEILLE after detecting the presence of R-ACK1, and only after waiting until ATU-R finishes sending R-ACK1.

12.2.4. C-ACT3

An alternate activate signal is reserved for future upgrades on initialization. C-ACT3 is similar to C-ACT1 and C-ACT2 except that $f_{C\text{-}ACT3}$ = 224.25 kHz. Referring to Figure 12.1.6, C-ACT3 is given by

$$X_k^n = X_k = \begin{cases} 0, k \neq 52, 0 \leq k \leq 256 \\ A_{C-ACT3}, k = 52 \end{cases}$$

$L_{C\text{-}ACT3}$ is also equal to 128 consecutive symbols with no cyclic prefix, with transmit power level equal to -4 dBm for the first 64 symbols and -28 dBm for the second 64 symbols.

12.2.5. C-ACT4

A fourth activate signal is also reserved for future upgrades on initialization. C-ACT4 is also similar to C-ACT1 except that $f_{C\text{-}ACT4}$ = 258.75 kHz. Referring to Figure 12.1.6, C-ACT4 is given by

$$X_k^n = X_k = \begin{cases} 0, k \neq 60, 0 \leq k \leq 256 \\ A_{C-ACT4}, k = 60 \end{cases}$$

$L_{C\text{-}ACT4}$ is also equal to 128 consecutive symbols with no cyclic prefix, with transmit power level equal to -4 dBm for the first 64 symbols and -28 dBm for the second 64 symbols.

12.3. Acknowledgment (ATU-R)

Similar to the ATU-C, there are vaious stages of initialization that results in errors (malfunction, timeout, insufficient margin, to name a few) and will come back to R-QUIET1 (occasionally R-ACT-REQ) for retraining. Again, some kind of external or internal monitoring may be required to keep track of which state did the ATU-R came back from. An example of an overall state diagram is shown in Annex A.

12.3.1. R-ACT-REQ

R-ACT-REQ is used when it is desirable for ATU-R to initiate a communication link to the ATU-C. For example, when a customer at ATU-R requests a service. R-ACT-REQ is transmitted after power-up and optionally a successful self-test (see Annex A). R-ACT-REQ is a single sinusoid at $f_{R\text{-}ACT\text{-}REQ}$ = 51.75 KHz and is given by

$$X_k^n = X_k = \begin{cases} 0, k \neq 12, 0 \leq k \leq 32 \\ A_{R-ACT-REQ}, k = 12 \end{cases}$$

where $A_{R\text{-}ACT\text{-}REQ}$ is an appropriate level so that the transmit power level is at -10 dBm (approximately -46 dBm/Hz over 4.3125 KHz) for the first 64 symbols and -30 dBm for the second 64 symbols. This signal is transmitted for $L_{R\text{-}ACT\text{-}REQ}$ = 128 consecutive symbols. R-QUIET1 follows immediately after R-ACT-REQ.

12.3.2. R-QUIET1

After transmitting R-ACT-REQ, the ATU-R enters the state R-QUIET1. Similar to all other quiet states, R-QUIET1 is a silent signal that is defined by

$$R-QUIET1 = X_k^n = X_k = \{0, 0 \leq k \leq 32$$

The duration of R-QUIET1, $L_{R\text{-}QUIET1}$, depends on whether the ATU-R receiver detects C-ACT1 (or C-ACT2) and how many times R-ACT-REQ has been transmitted. If the ATU-R receiver has not detected the presence of C-ACT1 or C-ACT2 for 4096 consecutive DMT symbol periods, then the ATU-R transmitter returns to R-ACT-REQ and

retransmit. If after the second R-ACT-REQ is sent, the ATU-C still fails to generate a C-ACT1 (or C-ACT2), then the ATU-R stays in R-QUIET1 indefinitely until either a reset (power-up), a detection of C-ACT1 (or C-ACT2), or some other commands (see Annex A). Successful detection of C-ACT1 (or C-ACT2) at ATU-R receiver triggers the ATU-R to move on to R-ACK1, immediately after C-ACT1 (or C-ACT2) signal ceases to transmit.

12.3.3. R-ACK1

As the counterpart of C-ACT1 (or C-ACT2), R-ACK1 is transmitted by ATU-R to continue initiating a communication link to the ATU-C. It serves as an acknowledgment to the detection of C-ACT1 (or C-ACT2). R-ACK1 is a single sinusoid at $f_{\text{R-ACK1}}$ = 25.875 KHz and is given by

$$X_k^n = X_k = \begin{cases} 0, k \neq 6, 0 \leq k \leq 32 \\ A_{R-ACK1}, k = 6 \end{cases}$$

where $A_{\text{R-ACK1}}$ is an appropriate level so that the transmit power level is at -10 dBm (approximately -46 dBm/Hz over 4.3125 KHz) for the first 64 symbols and -30 dBm for the second 64 symbols. This signal is transmitted for $L_{\text{R-ACK1}}$ = 128 consecutive symbols. R-QUIET2 follows immediately after R-ACK1.

12.3.4. R-ACK2

For future enhancement of initialization, R-ACK2 is reserved as the counterpart of C-ACT3. R-ACK2 at $f_{\text{R-ACK2}}$ = 34.5 kHz is similar to R-ACK1 and is defined as

$$X_k^n = X_k = \begin{cases} 0, k \neq 8, 0 \leq k \leq 32 \\ A_{R-ACK2}, k = 8 \end{cases}$$

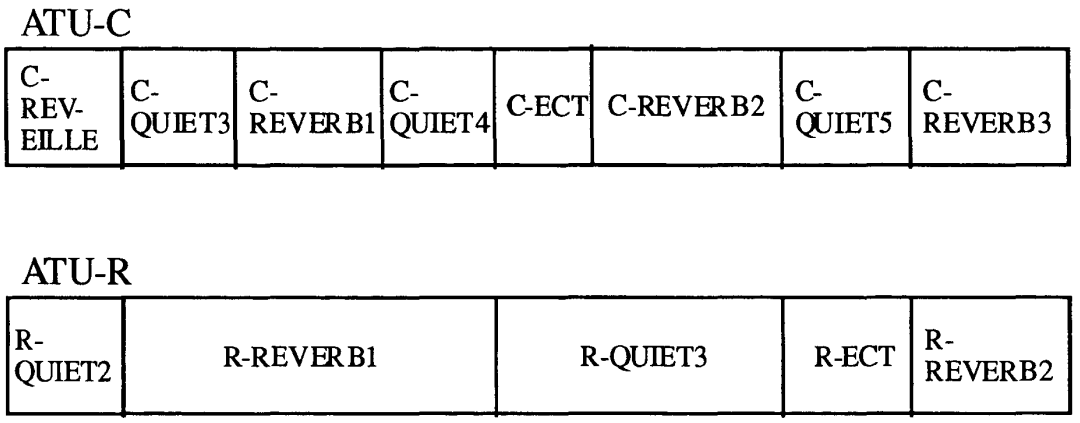
where the length and the transmit power level of R-ACK2 is the same as R-ACK1.

12.3.5. R-ACK3

For future enhancement of initialization, R-ACK3 is also reserved as the counterpart of C-ACT4. R-ACK3 at $f_{\text{R-ACK3}}$ = 43.125 kHz is similar to R-ACK1 and is defined as

$$X_k^n = X_k = \begin{cases} 0, k \neq 10, 0 \leq k \leq 32 \\ A_{R-ACK3}, k = 10 \end{cases}$$

where the length and the transmit power level of R-ACK3 is the same as R-ACK1.



(Drawn Not to Scale)

Figure 12.1.3 Timing Diagram of Transceiver Training (12.4-12.5)

12.4. Transceiver Training (ATU-C)

This and the next section describe the signal transmitted during transceiver training at ATU-C and ATU-R, respectively. Both ATU-C and ATU-R rely on counting the number of symbols starting at the beginning of transceiver training. Thus C-REVEILLE always coincides with R-QUIET2, C-QUIET5 coincides with R_ECT and so on. As a timeout feature throughout initialization, no states in Transceiver Training is allowed to be resided in continuously for more than 8000 symbols. If that occurs, the ATU-C will reset to C-ACT1 (or C-ACT2).

12.4.1. C-REVEILLE

C-REVEILLE, similar to C-ACT1, is a single frequency sinusoid at $f_{\text{C-REVEILLE}} = 241.5$ kHz. Using Figure 12.1.6, C-REVEILLE is given by

$$X_k^n = X_k = \begin{cases} 0, k \neq 56, 0 \leq k \leq 256 \\ A_{C-REVEILLE}, k = 56 \end{cases}$$

where $A_{\text{C-REVEILLE}}$ is an appropriate level so that the transmit power level is -4 dBm for the first 64 symbols, and -28 dBm for the second 64 symbols. C-REVEILLE is transmitted for $L_{\text{C-REVEILLE}} = 128$ consecutive symbols without cyclic prefix. C-REVEILLE is used as an acknowledgment of the detection of R-ACK1 and as a transition to C-QUIET3.

12.4.2. C-QUIET3

C-QUIET3 is a silent signal that is defined as

$$C-QUIET3 = X_k^n = X_k = \{0, 0 \leq k \leq 256$$

The duration of C-QUIET3, $L_{\text{C-QUIET3}}$, is equal to 512 symbols. C-REVERB1 follows C-QUIET3.

12.4.3. C-REVERB1 (Reverberation)

C-REVERB1 is a signal that allows the receiver at ATU-R to adjust its receive AGC to the appropriate level. C-REVERB1 is based on the psuedo-random binary sequence (PRBS) generated by the primitive polynomial,

$$p(D) = 1 + D^4 + D^9$$

with initial condition = 111111111. We apply the PRBS to each sub-carrier, X_k, k=0 to k=256 in succession. We group D.C. (k=0) and Nyquist (k=256) together for encoding the signal and treat them as the first sub-carrier. Thus if we define the bit stream out of the PRBS generator as:

p1p2p3p4p5p6..... ,
then the first (odd) bit of each pair of bits determines the polarity of the imaginary part of the sub-carrier and the second (even) bit determines the polarity of the real part. Specificially,

(p_{2k}, p_{2k-1})	Constellation (real, imaginary)
(0,0)	(+,+)
(0,1)	(+,-)
(1,0)	(-,+)
(1,1)	(-,-)

Table 12.4.1 Mapping to 4 QAM signal constellation

where p_1 maps to the real component of Nyquist tone, p_2 maps to the real component of D.C. tone, (p_4, p_3) maps to sub-carrier 1 (k=1), and so on. The signal level is chosen to conform with any appropriate power mask.
The pilot tone (tone #64 at 276 kHz) is overwritten by the (+,+) signal constellation with the appropriate signal level. During the previous segment (C-QUIET3 and R-REVERB1) the ATU-C estimates the received power level based on R-REVERB1 and then decides what transmit power level it will use from C-REVERB1 on. The mechanism to determine the appropriate ATU-C transmit power throughout initialization (starting from C-REVERB1) is TBD. The length of C-REVERB1, $L_{C\text{-}REVERB1}$, is equal to 512 (repeating) symbols without cyclic prefix. C-QUIET4 follows immediately after C-REVERB1.

12.4.4. C-QUIET4

C-QUIET4 is also a silent signal that is defined as

$$C-QUIET4 = X_k^n = X_k = \{0, 0 \le k \le 256$$

The duration of C-QUIET4, $L_{C\text{-}QUIET4}$, is equal to 3072 symbols. C-ECT follows C-QUIET4.

12.4.5. C-ECT

C-ECT is a vendor-defined signal that is intended to train the echo canceller at ATU-C for EC versions. Vendors of FDM versions have absolute freedom to define C-ECT signal. However, the length of C-ECT, $L_{C\text{-}ECT}$, is fixed at 512 DMT symbols. The receiver at ATU-R ignores this signal. C-REVERB2 follows C-ECT.

12.4.6. C-REVERB2

C-REVERB2 is a signal that allows the ATU-R receiver to perform synchronization and to train any receiver equalizer. C-REVERB2 is the same signal as C-REVERB1 (see Section 12.4.3). The length of C-REVERB2, $L_{C\text{-}REVERB2}$, is equal to 1536 (repeating) symbols without cyclic prefix. C-QUIET5 follows immediately after C-REVERB2.

12.4.7. C-QUIET5

C-QUIET5 is a silent signal that is defined as